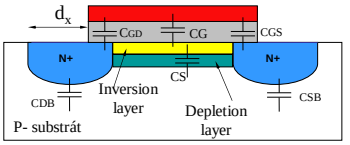
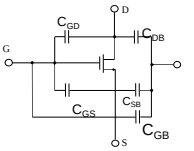
Electronics and Microelectronics
AE4B34EM

8. Lecture
- Unipolar transistor II
- Parameters
- Applications

MOS Device Capacitances





$$C_G = WLC_{ox}$$

$$C_S = WL\sqrt{q\varepsilon_r\varepsilon_0 N_A/(4\Phi_f)}$$

$$C_j = \frac{C_{j0}}{\left[1+V_R/\Phi_B\right]^m}$$

$$C_{DB} = C_{SB} = Wd_xC_j + 2(W+d_x)C_{jsw}$$

MOS Device Capacitances

Switchoff MOS

$$C_{GD} = C_{GS} = C_{ov}W$$

$$C_{GB} = \frac{WLC_{ox}C_2}{WLC_{ox}+C_2}$$

MOS in triode region when *VDS << 2 (VGS – Vt0)*

$$C_{GD} = C_{GS} = WLC_{ox}/2 + WC_{ov}$$

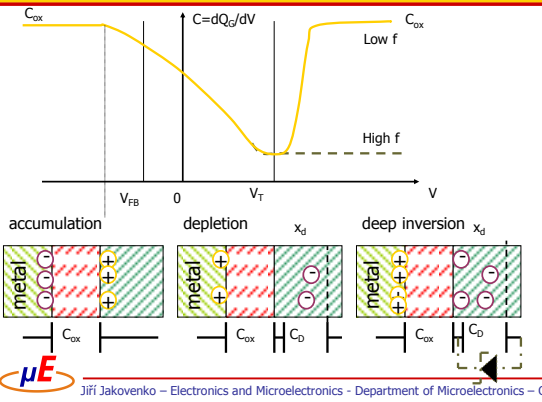
MOS in active region

$$C_{GS} = \frac{2}{3}WL_{eff}C_{ox} + WC_{ov}$$

Important constants:

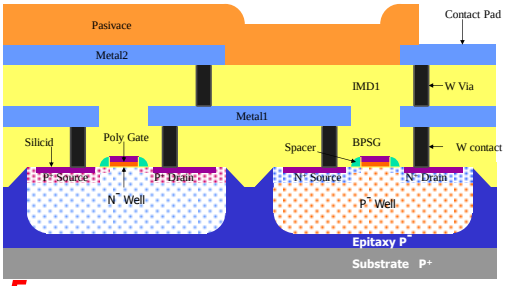
q = 1.602e^{-19} C	*k = 1.38e^{-23} JK^{-1}*
n_i = 1.1e^{16} carriers/m³ at T=300° K	*ε_0 = 8.854e^{-12} F/m*
Oxide ε_r = 3.9	*Silicon ε_r = 11.8*

C-V Characteristics

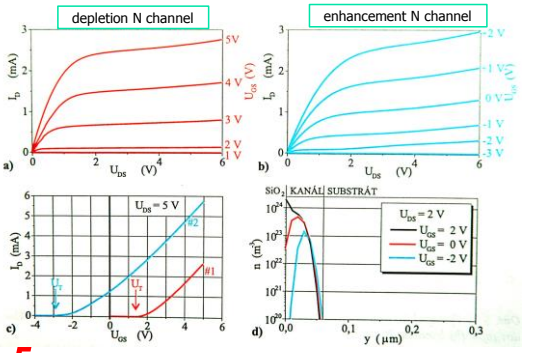


CMOS structure

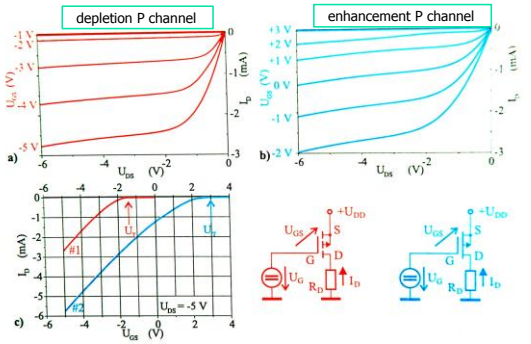
Complementrary MOS



Enhancement and depletion channel NMOS

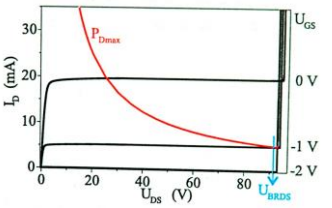


Enhancement and depletion channel NMOS



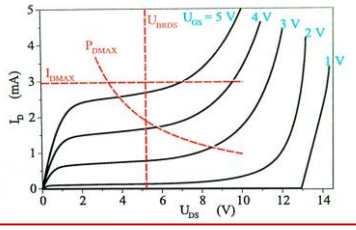
Limiting parameters of JFET

- Breakdown voltage V_{DS}
- Maximal power dissipation P_{Dmax}
- Maximal Gate current I_G



MOSFET Limiting parameters

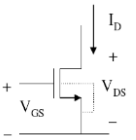
- Breakdown voltage V_{DS}
- Maximal power dissipation P_{Dmax}
- Maximal Gate voltage V_{GS}
- Maximal Drain current I_D



MOSFET application

Current mirrors and amplifiers

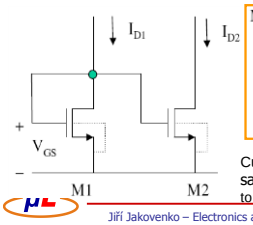
Current mirror



Assume that the transistor is in saturation

$$I_D = \frac{\mu_n C_{OX}}{2}\frac{W}{L}(V_{GS}-V_T)^2(1+\lambda V_{DS})$$

$$V_{GS} = V_T + \sqrt{\frac{2I_D}{\frac{\mu_n C_{OX}}{2}\frac{W}{L}(1+\lambda V_{DS})}}$$



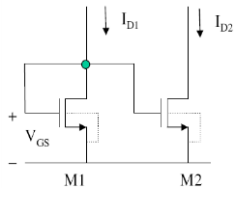
M1=M2 =>

$$I_{D1} = \frac{\mu_n C_{OX}}{2}\frac{W}{L}(V_{GS}-V_T)^2(1+\lambda V_{DS1})$$

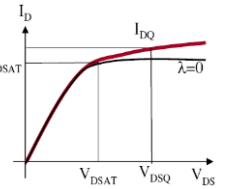
$$I_{D2} = \frac{\mu_n C_{OX}}{2}\frac{W}{L}(V_{GS}-V_T)^2(1+\lambda V_{DS2})$$

Current I_{d1} sets the voltage V_{GS}, which is same for both transistors. Thus I_{d2} must be equal to I_{d1}

Current mirror

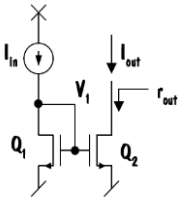


$$I_{D2}=\frac{\mu_n C_{OX}}{2}\left(\frac{W}{L}\right)_2(V_{GS}-V_{T2})^2=\frac{\mu_n C_{OX}}{2}\left(N\frac{W}{L}\right)_1(V_{GS}-V_{T2})^2\ I_{DSAT}$$

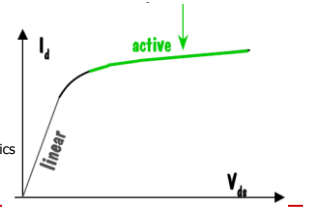


CMOS Current mirror

- ***Applications:***
  - *Power supply*
  - *Current Multiplier*
  - *Active load with a high resistance*

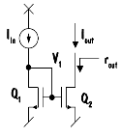


$$I_{ds}(sat)=\frac{W}{2L}\mu_n C_{ox}(V_{gs}-V_t)^2$$



Both transistors have the same characteristics
The transistors in active mode

Operational principle



$$I_{D2}=\frac{\mu_n C_{OX}}{2}\left(\frac{W}{L}\right)_2(V_{GS}-V_T)^2(1+\lambda_2 V_{DS2})$$

$$I_{D2}=\frac{\frac{\mu_n C_{OX}}{2}\left(\frac{W}{L}\right)_2(V_{GS}-V_{T2})^2(1+\lambda_2 V_{DS2})}{\frac{\mu_n C_{OX}}{2}\left(\frac{W}{L}\right)_1(V_{GS}-V_{T1})^2(1+\lambda_1 V_{DS1})}I_{D1}=\frac{K_{P2}(V_{GS}-V_{T2})^2(1+\lambda_2 V_{DS2})}{K_{P1}(V_{GS}-V_{T1})^2(1+\lambda_1 V_{DS1})}NI_{D1}$$

Error: $\approx \lambda_2 V_{DS2}-\lambda_1 V_{DS1}$

$$\lambda \propto \frac{1}{L}$$

Increasing the length of the channel reduces Current Mirror error inaccuracies

Error: $\approx K_{P2}-K_{P1}$

Error: $\approx V_{T2}-V_{T1}$

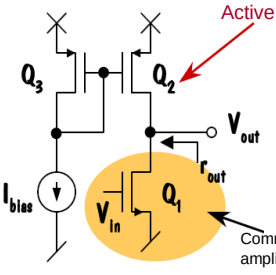
Error can be minimized by proper layout

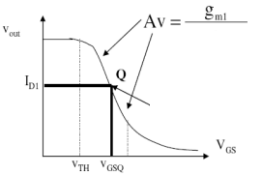
CMOS amplifiers stages

Common source amplifier

- Most common amplifier stage, especially when required high output resistance
- Active load provides high-impedance loads without using high levels of resistance or high voltage supply
- With active load we can get higher gain
- Eg.: 1MΩ load and 100 mA current requirement, we would need 1MΩ x 100mA voltage = 100V

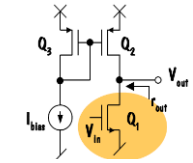
Common source amplifier





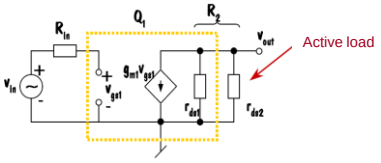
Common source amplifier Small signal model

Transistors Q2 and Q3 must be in active mode



$$v_{gs1} = v_{in}$$

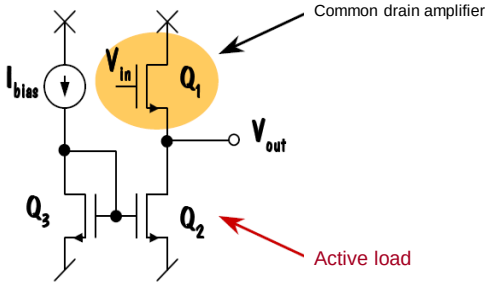
$$A_v = \frac{v_{out}}{v_{in}} = -g_{m1}R_2 = -g_{m1}\left(r_{ds1} \| r_{ds2}\right)$$



Common drain amplifier (Voltage follower)

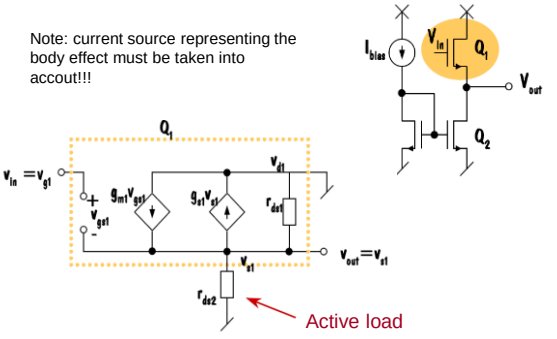
- The most common use - the voltage buffer (voltage follower)
- Voltage gain is ideally close to one
- Current gain >> 1
- DC input voltage level is not the same as the output
- The gain limiting factor is the body effect

Common drain amplifier

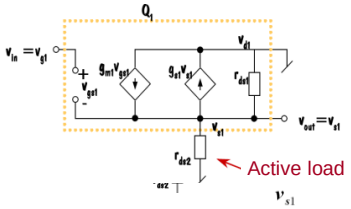


Common drain amplifier Small signal model

Note: current source representing the body effect must be taken into accout!!!



Common drain amplifier Small signal model



g_{s1} is usually 5-10% of gm1, g_{ds1} and g_{ds2} are 1/10 of g_{s1}

Body effect is the main reason why the voltage gain is less than one

$$v_{out}\left(g_{ds1} + g_{ds2}\right) + g_{s1}\underbrace{v_{out}}_{v_{s1}} - g_{m1}\left(v_{in} - v_{out}\right) = 0$$

$$A_v = \frac{v_{out}}{v_{in}} = \frac{g_{m1}}{g_{m1} + g_{s1} + g_{ds1} + g_{ds2}}$$

Common gate amplifier

- Common gate amplifier exhibits low input resistance
- Example:
  - *Data lines Terminator with input impedance of 50Ω*
  - *The first amplifier stage where it is necessary to amplify current*

Common gate amplifier