10. lecture
- IC processing technology
- Lithography
- Oxidation
- Ion Implantation
- Deposition

How to get 1,000,000,000 Components to 1 cm²

Transfer of the design on a chip

Photolithography - projection method

Photolithography and etching

Photolithography
- Today we use UV light sources of 248, 195nm
- Very expensive equipment 40,000,000 USD
Resolution Enhancement Techniques

Resolution Enhancement Techniques

GDSII

MDP

Mask Manufacturing

OPC – Optical proximity correction

Resolution enhancement techniques

Design

180nm

130nm

90nm and Below

Mask

OPC

Wafer

Feature sizes

light wavelength

OPC – Optical proximity correction

PSM – Phase shift mask

Source: IDESA

Optical Proximity Correction

Predistortion of the mask layout is needed when scaling down the technology

No OPC

OPC Corrections

With OPC

Original Layout

Needed for 90nm and below

Source: IDESA

Optical Proximity Correction

Increasing percent of mask layers are using OPC/RET technologies

% of RET

Technology Node (nm)

Source: IDESA

Optical Proximity Correction

Comparison by difference of OPC method

Original

Moderate

Aggressive

Source: IDESA

Optical Proximity Correction: Mask Writing Time

Number of Shots by E-beam used in electron lithography (Giga)

Source: IDESA
**Phase shift mask**

- **Light phase shifting**
- **Conventional Mask**
- **Alternating PSM**

**Design**

- **Cross Section**
- **Electric Field**
- **Sum**
- **Intensity**

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**Immersion photolithography**

- Technique which improves resolution photolithography resolution (30-40%)
- **DUVI** – use liquid between the lens system and wafer
  - This will increase the depth of field (DOF)
  - NA value is significantly greater than 1.0
  - Use absolutely clean water
- Necessary for technology node 45 nm (ASML, Canon and Nikon)
- There are solutions for 14 nm technology (Intel Ivy Bridge)

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**EUV Extreme ultraviolet lithography**

- Radiation source 13.5 nm
- Requires vacuum
  - All optics (mirrors) including masks must be made of multilayer Mo / Si without fault

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**Etching process - basic types**

- **Wet chemical etching**
- **Plasma etching**
- **Reactive ion etching**
Anisotropic and isotropic etching

- **Anisotropic etching**
  - Anisotropy coefficient: \( A_f = 1 - \frac{V_H}{V_V} \)
- **Isotropic etching**
  - Isotropic etching is coefficient: \( A_f = 0 \)

Selectivity to resist: \( S_{RM} = \frac{V_F}{V_M} \)
Selectivity to wafer: \( S_{FS} = \frac{V_F}{V_S} \)

**Plasma etching**

- Used for silicon-nitride layers and photoreist remover.
- The process uses a high reactive fluorine atoms which is generated by the decay of Freon \( CF_4 \) molecules at very high temperature and mixed with oxygen are used.

**Thermal oxidation**

- The thin layer of oxide are created on air (1 - 2 nm).
- At higher temperature (800°C - 1200°C) oxygen molecules are able to diffuse through oxide layer. 44% thickness is below the original surface of silicon and 56% above.

**Oxidation (diffusion) chamber**

- Temperature inside the chamber is 400 - 1200°C.
- The tube is made of quartz glass.

**Local oxidation masked by Silicon-Nitride**

- a) Nitride deposition: It serves as an oxidation mask.
- b) Transferred on masks: Nitride is etched.
- c) Local oxidation.
- d) Local oxidation masked by Silicon-Nitride.
**Ion Implantation**

Ion implantation is a process in which dopant atoms are implanted below the surface of the silicon wafer. Dopant ions are accelerated by an electric field and focused to the wafer surface where they penetrate to a certain depth beneath the surface of silicon.

**Diffusion - the principle**

Diffusion is one of the most common processes in nature. Diffusion rate is strongly dependent on temperature. At high temperatures diffusion is used in semiconductor process for localised doping.

**Diffusion in semiconductor process**

In this process dopant atoms penetrate below the silicon surface in selected areas. Temperature and time adjust layer depth and dopant concentration on the surface.

**Annealing** is the mechanism by which the dopant atoms in silicon move around without diffusion source. It positively forms dopant profile. Oxide on the surface of the silicon wafer must be sufficiently thick (about 500 nm) to stop atoms of phosphorus penetrating through it.

**An Ion implantation system**

Electric discharge source breaks the molecules into phosphorus and chloride atoms or clusters of atoms with an electric charge. The ions are accelerated by the accelerator.

**Shallow (Silicone) trench isolation - STI**

STI - Shallow Trench Isolation

- Oxide and nitride Si$_3$N$_4$ deposition
- Masked etching Si$_3$N$_4$ and SiO$_2$
- CMP grinding of carbon nitride layer
- Removal of nitride by (H$_3$PO$_4$)
- etching Si
- SiO$_2$ deep $x \sim 250$ nm, "shallow"

Oxide deposition fills the trench etched (it's thermal oxide?)

**Dopant profile changes during annealing.**

The quantity of dopants is an important parameter called the *dose*. The quantity of dopants is an important parameter called the *dose*. The ion source. Positive ions of P and Cl. Phosphorus (P). Si wafer doped by Phosphorus has a N type conductivity.
Ion implantation – Magnet system

Ion implantation – Magnet system

Accelerator system

Accelerator system

Linear accelerator system

Linear accelerator system

Electron shower system

Electron shower system

Epitaxial growth

Epitaxial growth

Sputtering

Sputtering
**Sputtering system**

The target is connected to the negative pole of the high voltage source and the auxiliary electrode— anode — to the positive pole. Argon atoms are ionized and discharged and accelerated by an electric field and directed at the target. Sprayed aluminium target is deposited on the plates, creating a layer of aluminium. The magnetic field located behind the target increases the efficiency of sputtering process.

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**Chemical Vapor Deposition CVD**

- $\text{SiH}_4(gas) + \text{O}_2(gas) \rightarrow \text{SiO}_2$ (solid) + $2\text{H}_2$ (gas)
- $\text{SiH}_4(gas) + \text{H}_2(gas) + \text{SiH}_2(gas) \rightarrow 2\text{H}_2(gas) + \text{PolySilicon}$ (solid)

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**Metalization – conductive couplings**

- Today Al is substituted by Cu — 40% less resistivity
- Maximum 11 metal layers

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**CMP – Chemical-mechanical planarization**

- Chemical-mechanical planarization / Polishing
  - Mechanically with chemical etching, or chemically with mechanical grinding ...
  - ... why? — surface planarization with removal of excess material

- Chemical reaction etches surface and makes the deposited material soft, then the mechanical grinding flattens the surface.

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**CMP – Chemical-mechanical planarization**

Suspension = chemicals + particles

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IC testing process

- Optical control
- Measurements of test structures

Packaging

Package requirements:

- Electrical – small parasitic capacitances, inductance
- Mechanical – reliable and solid
- Thermal – good heat dissipation
- Economical - cheap

Packaging

Diamond saw cuts the silicon wafer with chips into individual chips. Good chips are soldered or glued into the case. Leads are connected to contacts on the chip with a thin copper wire (0.15 mm).

Board mounting

(a) Through-Hole Mounting  (b) Surface Mount

Package types

Package parameters

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Capacitance (pF)</th>
<th>Inductance (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>60 Pin Plastic DIP</td>
<td>4</td>
<td>10</td>
</tr>
<tr>
<td>60 Pin Ceramic DIP</td>
<td>7</td>
<td>20</td>
</tr>
<tr>
<td>256 Pin Gold Lead</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>Wire Bond</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Solder Bump</td>
<td>0.5</td>
<td>0.1</td>
</tr>
</tbody>
</table>