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		REPRESENTATIVE DIVISION
	SPECIFICATION	☐ IC DIV. 0 SEMICONDUCTOR APPLICATION DIV. ■ LCD DIV. ☐ ELECTRONIC COMPONENTS DIV. ☐

DEVICE SPECIFICATION FOR

Dot Matrix LCD Unit
(20-character/2-line Display
STHC gray type)

MODEL No.

LM20A21

☐ CUSTOMER'S APPROVAL

DATE

BY

PRESENTED
BY

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SHARP COWOWTION

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LM20A21

1. Overview

The LM20A21, dot-matrix LCD unit consists of a 5 x 7-dot 20-character 2-line dot-matrix LCD panel, LCD driver and controller LSI fabricated on a single PCB. Incorporating mask ROM-based character generator and display data RAM in the controller LSI, the unit can efficiently display the desired characters under microprocessor control.

(Features)

(1) The LCD of the unit is STHC(Super Twisted High Contrast) gray type.

(2) Low power consumption with the dot-matrix LCD panel and CMOS LSI.

(3) Thin, lightweight design permits easy installation in a variety of equipment.

(4) Allowing for being connected at general-purpose CMOS signal level, the unit can be easily interfaced to a microprocessor with common 4-bit and 8-bit parallel inputs and outputs.

(5) Built-in character generator ROM and RAM, and display data RAM:

Character generator ROM
160 different 5 x 7 dot-matrix character patterns
(Alphanumeric and symbols)

Character generator RAM
8 different user programmed 5 x 7 dot-matrix patterns

Display data RAM
80 x 8 bits

(6) Numerous instructions
Display clear, Cursor home, Display ON/OFF, Cursor ON/OFF, Blink character, Cursor shift, Display shift

(7) Built-in reset circuit is triggered at power ON.
(For the operating conditions, refer to the separate user's manual "Dot-Matrix LCD Units with built-in controllers".)

(8) The unit operates from a single 5V power supply.

* As to the packing, refer to the separate "COMMON PACKING SPECIFICATION FOR LM20255 series".

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2. Construction and Outline

Construction : 5 x 7 dots + cursor, 20-character 2-line dot-matrix display unit

Outline : See Fig. 7.

Interface signals : See Table 5.

Character pattern details : See Fig. 7.

Character codes : See Table 8.

There shall be no scratches, stains, chips, distortions and other externa drawbacks that may affect the display function.
Rejection criteria shall be noted in Inspection Standard (s-u- 009).

3. Mechanical Specifications

Table 1

Parameter	Specification	Unit
Outline dimensions	115(W) X 36(H) X11 MAX(D)	mm
Effective display area	83(W) X 18.6(H)	mm
Display format	20 characters X 2 lines	
Character format	5 X 7 dots with cursor	
Character size	3.2(W) X 4.85(H) (5 X 7 dots)	mm
Dot size	0.6(W) X 0.65(H)	mm
Dot spacing	0.05	mm
Character color *	Dark blue	
Background color*	Gray	
Weight	Approx. 40	g

* Due to the characteristics of the LC Material, the colors vary with environmental temperature.

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4. Electrical Specifications

4.1 Absolute maximum ratings

Table 2

Parameter	Symbol	Hin.	Max.	Unit	Remark
Supply voltage(Logic)	$V_{DD}-V_{SS}$	-0.3	+6.5	V	
Supply voltage(LCD drive)	V_0-V_{SS}	0	+6.5	v	$V_{DD}>V_0$
Input voltage	V_{IN}	-0.3	$V_{DD}+0.3$	V	
Storage temperature	Tstg	-25	+70	"C	
Operating temperature	Topr	o	+50	"C	

4.2 Electrical characteristics

Table 3 (Ta = 25℃)

Parameter		Symbol	Min.	Typ.	flax.	Unit	Condition
Supply voltage(Logic)		$V_{DD}-V_{SS}$	4.75	5.0	5.25	v	
Supply voltage (LCD drive)		V_0-V_{SS}		0.5		v	V_{DD}=5.0V
Input voltage	" L "	V_{IL}	-0.3	-	0.6	v	
	" H "	'IH	2.2	-	V_{DD}	v	
Output voltage	" L "	V_{OL}			0.4	v	I_{OL}=1.2mA
	" H "	V_{OH}	2.4	-	-	v	$-I_{OH}$=0..205mA
Input leakage current		I_{IL}			1	μA	
Internal oscillating frequency		fosc		250		KHz	
Supply current		I_{DD}		1.8	2.5	mA	V_{DD}=5V
Power dissipation		Pd		9	12.5	mW	V_0=0V

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4.3 Timing characteristics

Table 4

V_{DD}=5.0V±5%

Ta =0~50℃

Parameter	Symbol	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cycE}	1000	-	-	ns
Enable pulse width	PW_{EH}	450	-	-	ns
Enadle rise/fall time	t_{Er}, t_{Ef}	-		25	ns
RS, R/W setup time	t_{AS}	140	-	-	ns
Address hold time	tAH	10	-	-	ns
Data setup time	t_{DSW}	195	-	-	ns
Data delay time	t_{DDR}			320	ns
Data hold time (write)	t_H	10	-		ns
Data hold time(read)	tDHR	20	-	-	ns

Timing chart: See Fig. 1.

4.4 Interface signals

Table 5

Pin No.	Symbol	Description	Connection
1	V_{SS}	Ground potential	GND : OV
2	V_{DD}	Power supply	+5V
3	V_0	Contrast adjustment voltage	Adjust the contrast by changing the supply voltage from OV to 5V.
4	RS	Register select signal	Control signal inputs (For details, see section 6 and 7.)
5	R/W	Read/write select signal	
6	E	Operation(data read/write enable signal)	
7	DB_0	Code 1/0 data LSB	Data bus line . DB_7 may also be used to check the busy flag. · Lines DB_0~DB_3 are not used when interfacing with a 4-bit microprocessor. (For details, see section 6 and 7.)
8	DB_1	Code I/O data 2nd bit	
9	DB_2	Code 1/0 data 3rd bit	
10	DB_3	Code I/O data 4th bit	
11	DB_4	Code I/O data 5th bit	
12	DB_5	Code I/O data 6th bit	
13	DB_6	Code I/O data 7th bit	
14	DB_7	Code I/O data MSB	

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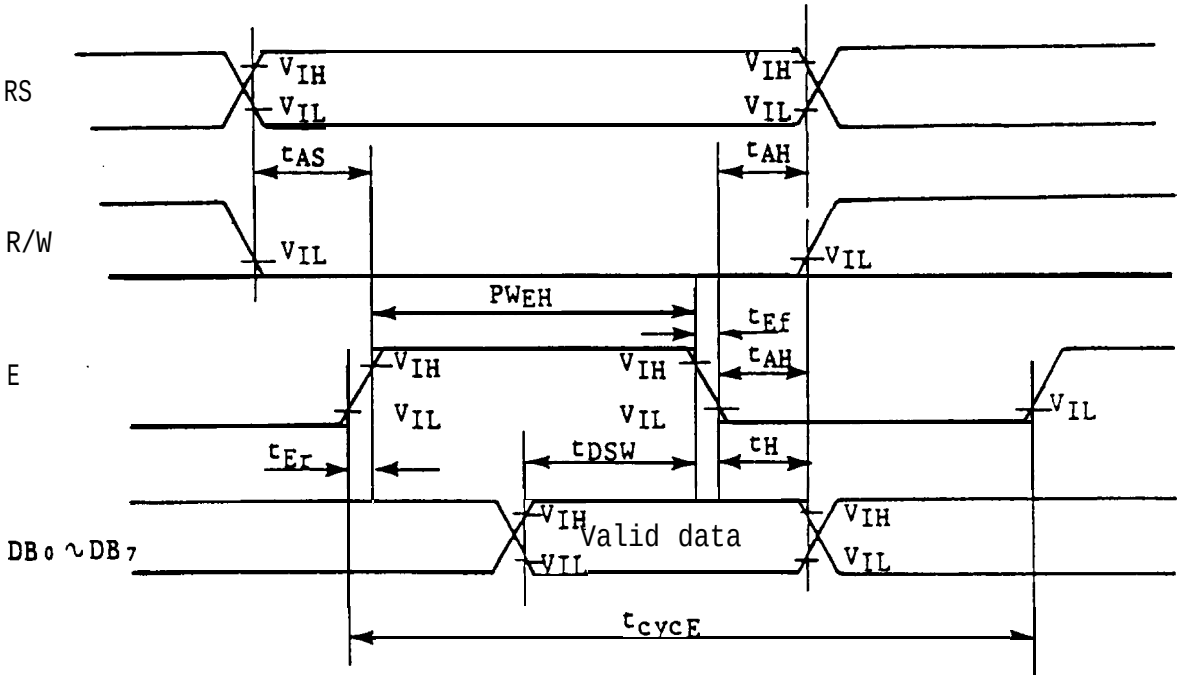
Write Operation



Read Operation

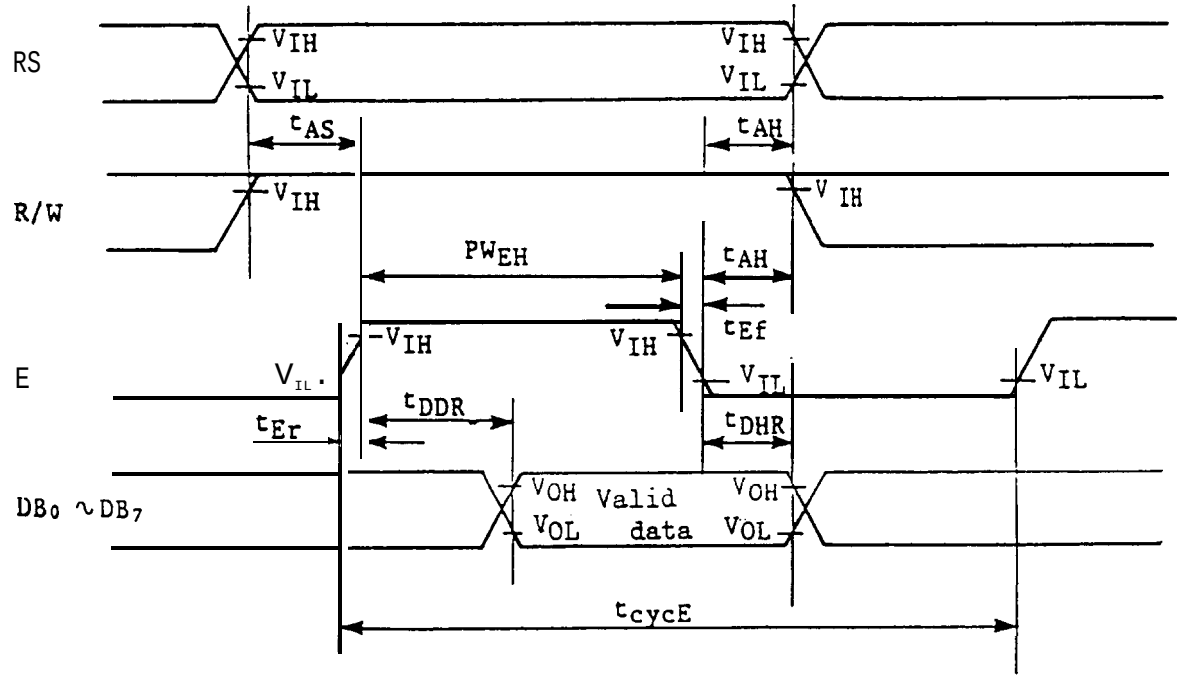


Fig. 1 Timing Chart

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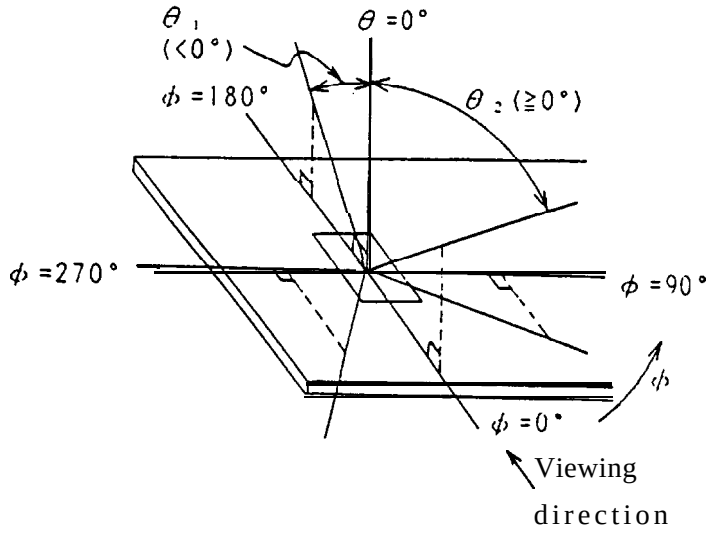
5. Optical Characteristics

Table 6 shows the optical characteristics when LCD drive voltage is adjusted to the maximum contrast in $\theta = 0°$.

Table 6 (Ta=25℃)

Parameter		Symbol	Condition		Min.	Typ.	Max.	Unit	Remark
Viewing angle range		$\theta_2-\theta_1$	ϕ=0"	$C_0 \geqq 2.0$	60	-		dgr.	Note 1
		θ_1	$\theta_1 < \theta_2$	C_0=2.0	-	-	-25	dgr.	Note I
		θ_2			25	-	-		
		$\theta_2-\theta_1$	ϕ=45"	$C_0 \geqq 2.0$	60	-	-	dgr.	Note 1
		θ_1	315"	C_0=2.0	-	-	-25	dgr.	Note 1
		θ_2	$\theta_1 < \theta_2$		25	-	-		
Contrast ratio		C_0	$\theta = 0°$, $\phi = 0°$		3.0	5.0	-		Note 2
Response time	Rise	t_r"	e =0" , $\phi = 0°$		-	150	250	ms	Note 3
	Decay	td	$\theta = 0''$, $\phi = 0°$		-	150	250	ms	Note 3

Note 1) The viewing angle range is defined as shown below.



* Angles θ_1, θ_2 and ϕ shall fall within the range over which the displayed character can be read.

Fig.2 Definition of viewing angle

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Note 2) Contrast ratio is defined as follows:

When input signal is applied to the unit to select (turn on) the LCD dots (pixels) to be measured in the optical characteristics test method as defined in Fig. 3.

$$\text{Contrast ratio} = \frac{\text{Photodetector output voltage with non-select waveform being applied}}{\text{Photodetector output voltage with select waveform being applied}}$$

Measurement wave length $\lambda = 580\,nm$

Note 3) When input signal for selecting or non-selecting the dots to be measured are applied using the optical characteristics test method shown in Fig. 3. The response characteristics of the photo-detector output are measured as shown in Fig. 4.

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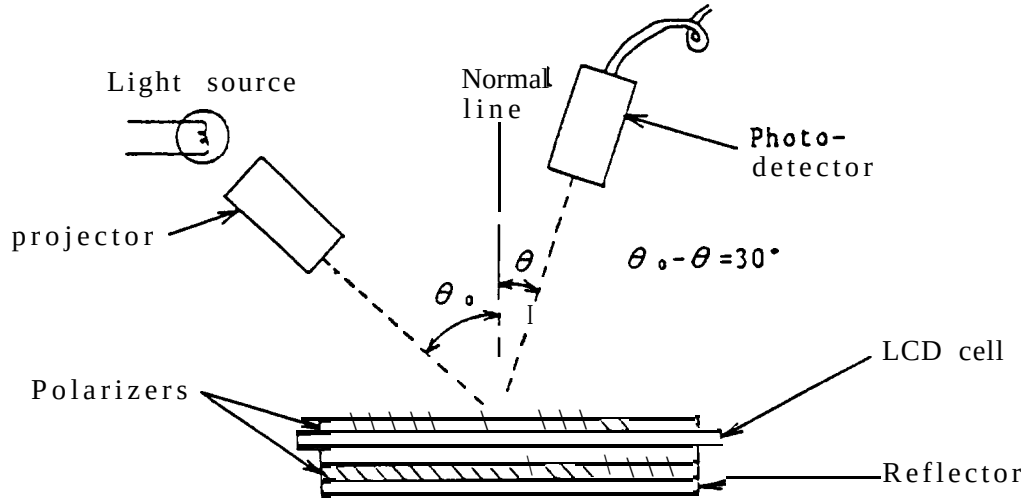


Fig. 3 Optical Characteristics Test Method

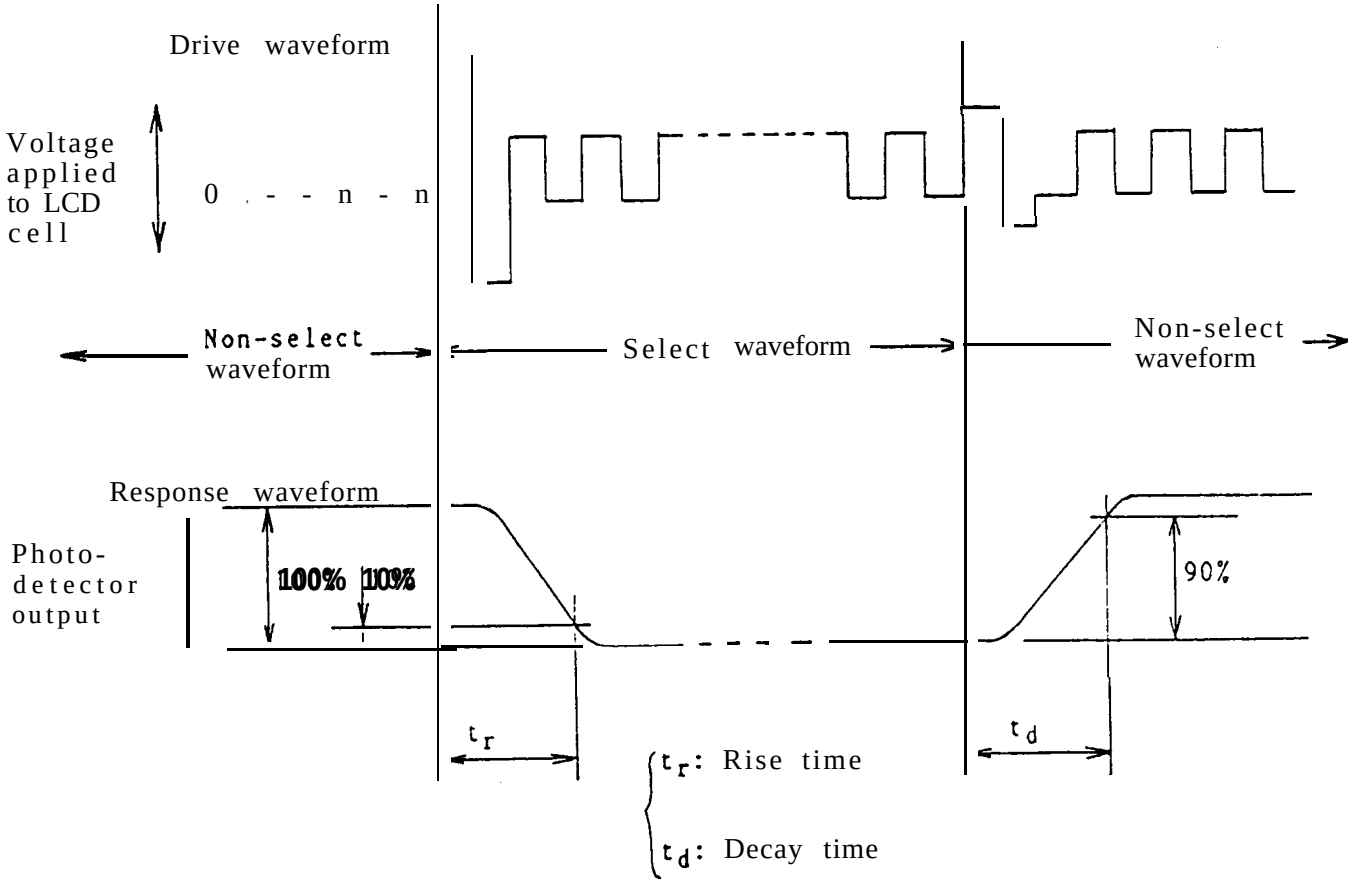


Fig. 4 Definition of Response Time

6. Pin Description

1) V_{DD} and V_{SS} Pins

V_{DD} and V_{SS} pins are for power supply. V_{SS} pin is "grounded,and V_{DD} pin is supplied with +5V. Each voltage necessary to drive LCD is generated in the unit.

2) RS Pin

The controller LSI has two 8-bit registers; an instruction register (IR) and a data register (DR). RS signal selects these registers.

IR stores instruction codes such as display clear, shift, etc. and also stores address information for the display data RAM (DD RAM), character generator RAM (CG RAM); DR is used for temporary ly'storing data to be written into DD RAM and CG RAM.

" O " :Instruction register (when writing)
Busy flag register; address counter (when reading)
" 1 " :Data register (read/write)

3 R/W Pin

Read or write select signal pin.

" O " :Writing
" I " :Reading

4) E Pin

Data read or write operation enable signal pin.

5) $DB_0 \sim DB_7$ Pins

Data bus with three-state, bidirectional function for use in data transactions with MPU. DB_7 may also be used to check the busy flag. $DB_0 \sim DB_3$ are not used when interfacing with a 4 - bit microprocessor.

6) V_0 Pin

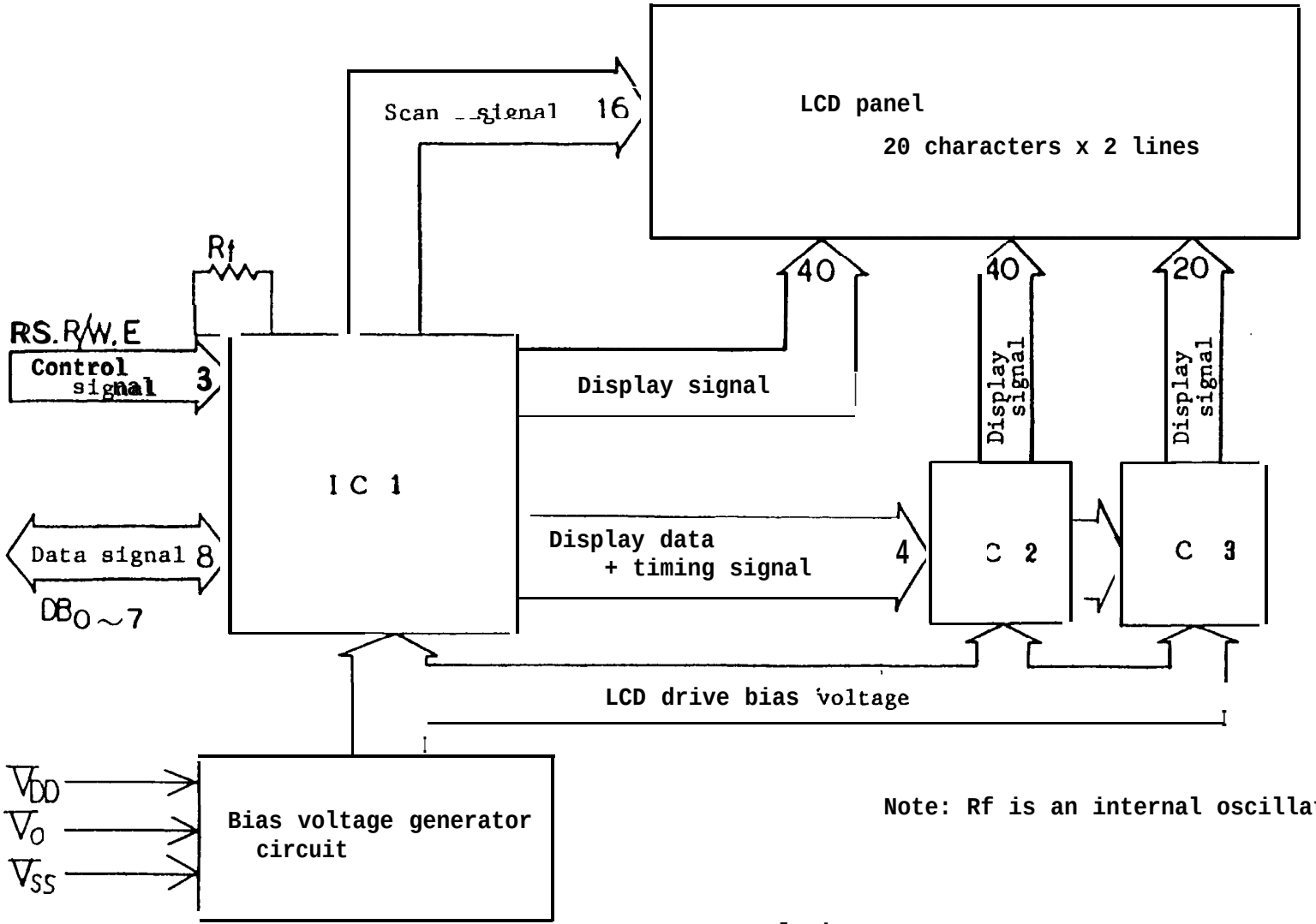
Viewing angle is varied and contrast is adjusted by changing voltage between +5V $\sim$ OV by applying bias voltage to the LCD driver.

7. Instruction Set

Table 7

Instruction	Code										Function
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB2	DB1	DBo	
Display clear	o	0	0	0	0	0	0	0	0	1	Clear entire display area, restore display from shift, and load address counter with DD RAM address 00_H.
Display/cursor home	o	0	0	0	0	0	0	0	1	•	Restore display from shift and load address counter with DD RAM address 00_H.
Entry mode set	0	0	0	0	0	0	0	1	I/D	s	Specify cursor advance direction and display shift mode. This operation takes place after each data transfer.
Display ON/OFF	o	0	0	0	0	0	1	D	c	B	specify activation of display (D), cursor(C), and blinking of character at cursor position (B).
Display/cursor shift	o	"o	o	0	0	1	S/C	R/L	•	*	Shift display or move cursor.
Function set	o	0	0	0	1	DL	1	0	*	•	Set interface data length (DL).
CG RAM address set	o	0	0	1	ACG						Load the address counter with a CC RAM address. Subsequent data is CC RAM data.
DD RAM address set	o	0	1	ADD							Load the address counter with a DD RAM address. Subsequent data is DD RAM data.
Busy flag/address counter read	o	1	BF	AC							Read busy flag (BF) and contents of address counter (AC).
CG RAM/DD RAM data write	1	0	Write data								Write data to CC RAM or DO RAN.
CC RAM/DD RAH data read	1	1	Read data								Resd data from CG RAM or DD RAN.

I/D-1: increment, I/D-O: Decrement
S = 1: Shift display, S -O: 'Freeze display
D = 1: Display ON, D -O: Display OFF
"C = 1: Cursor ON, c = O: Cursor OFF
B = 1: Character at cursor position blinks, B -O: Character at cursor position unblinks
SIC-1: Shift display, S/C = 0: Hove cursor
R/L-1: Shift right, R/L-O: Shift left
D L = 1: 8-bit, DL -O: 4-bit
BF = 1: During internal operation, BF -O: End of internal operation



Note: Rf is an internal oscillating resistor.

Fig. 5 Block Diagram

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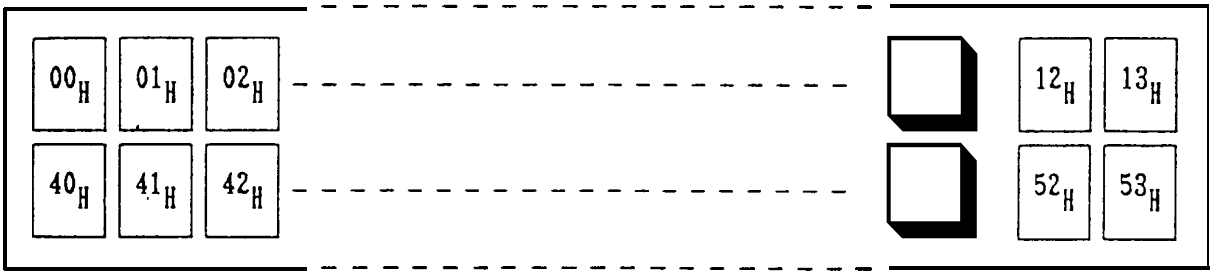

Fig.6 Display Address (When the display is not shifted)

Table 8 Input Code vs. Character Pattern

*2 4bit \ *1 4bit	0000	0010	0011	0100	0101	0110	0111	1010	1o11	1100	1101	1110	111
xxxx0000	CG RAM (1)												*
xxxx0001	(2)												*
xxxx0010	(3)											*	
xxxx0011	(4)												
xxxx0100	(5)											*	
xxxx0101	(6)												
xxxx0110	(7)											*	
xxxx0111	(8)											*	
xxxx1000	(1)												
xxxx1001	(2)												*
xxxx1010	(3)											*	
xxxx1011	(4)												
xxxx1100	(5)												
xxxx1101	(6)												
xxxx1110	(7)												
xxxx1111	(8)												*

Note 1. CG RAM Is character generator RAM in which user-definable character pattern are stored.

Note 2. X mark: prohibition of input

*1 High-order *2 Low-order

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設計通報 DRAWING INFO. 連絡書 INFORMATION

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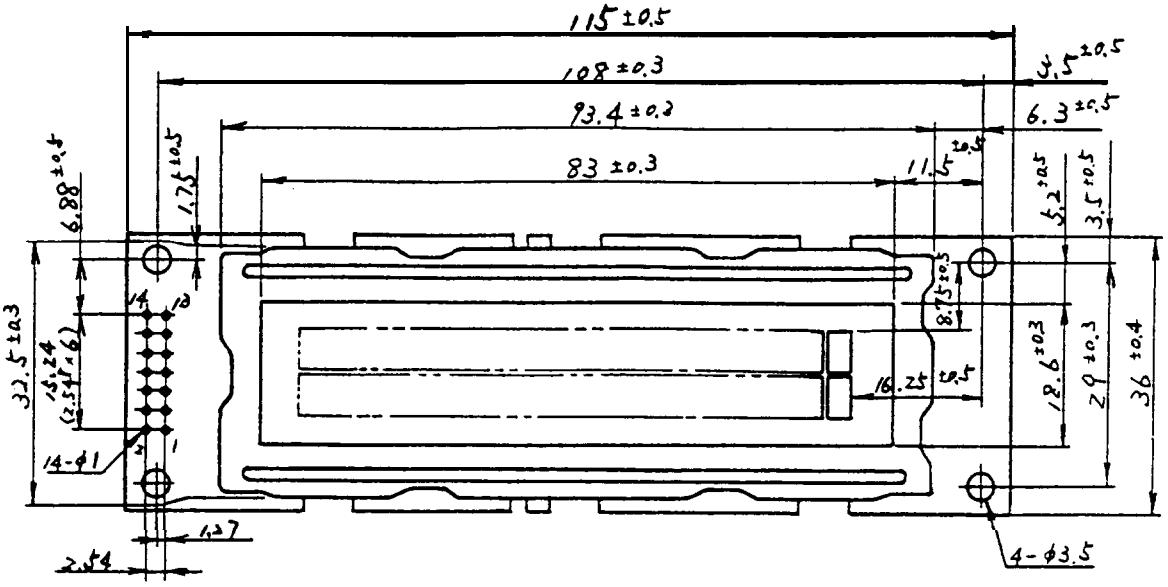
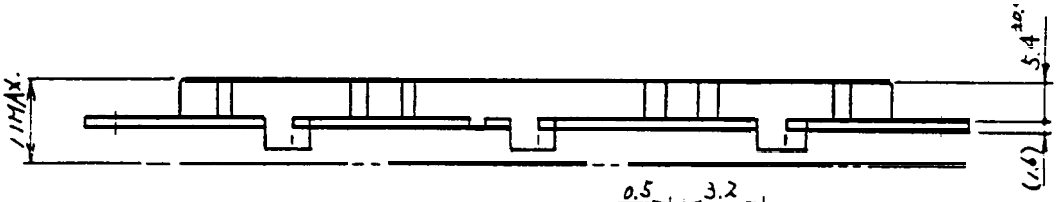
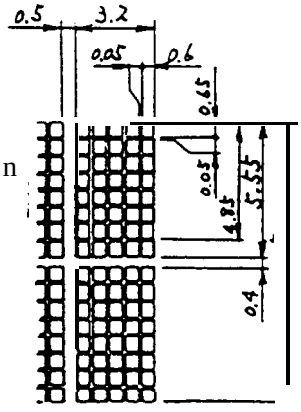
Fig.7 Unit Outline Dimensions and Pin Connections





PIN No.	Sig.	PIN No.	Sig.
14	DB7	13	DB6
12	DB5	11	DB4
10	DB3	9	DB2
8	DB1	7	DB0
6	E	5	R/W
4	RS	3	V0
2	VDD	1	VSS

Character Pattern Details



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	年月日 DATE	訂正記事 REVISE		設通No.	担当 PREPA	適用機種 MODEL

材質 MATERIAL	板厚 THICKNESS	仕上 FINISH	尺度 SCALE
			1/1

設計 DESIGN	写図 TRACE	検図 CHECK	検図 CHECK	承認 APPROVED
高岡		村岡	里アマ村	服六

シャープ株式会社
SHARP CORPORATION
発行部門 LCD Division

様式総 44－A 4

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記号 SYMBOL	
部品コード PARTS CODE	
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図番 DRAWING No.	OD20A21-301C