Materiály k přednášce
STM32 ARM® Cortex™-M3

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V rámci předmětu X38MIP
Katedra měření
České vysoké učení technické v Praze
Introducing the STM32

• STM32 reshapes the Microcontroller Market
  – First MCU family eliminating all obstacles to broad 32-bit usage
  – First ARM® Cortex™-M3 MCU family from a leading semiconductor supplier
  – Worlds largest Cortex-M3 portfolio
  – Strongest, Most Diverse roadmap for future developments

• The STM32 family brings new degrees of freedom to MCU by combining:
  – Leading performance
  – Real-time behavior
  – Outstanding power efficiency
  – First-class peripherals
  – Maximum integration
  – Excellent tools and software ecosystem
STM32, An MCU Without Constraints

- **High performance “Cortex-M3” core from ARM**
  - 1.25 Dhrystone MIPS/MHz vs 0.95 for ARM7TDMI

- **First-class peripherals**
  - 1µs triple 12-bit ADC, 4.5Mbit/s USART, 18Mbit/s SPI, SDIO, I2S, DAC, FSMC

- **Low power / Low voltage**
  - As low as to 27mA at 72MHz and down to 1.1µA in backup mode
  - Single supply 2.0V to 3.6V

- **Maximum integration**
  - Reset circuitry, LVD, voltage regulator, accurate RC oscillator

- **Simple architecture and easy-to-use tools**
  - From ST, IAR, Keil, Micrium, ThreadX, Greenhills, DataI/O, etc

- **Accessible**
  - Access Line 256KB Flash, 64 pins, resale price : $3.72 (10Ku)
  - Performance Line 512KB, 144 pins, resale price : $6.51 (10Ku)
  - Access Line 16KB Flash, 36 pins, resale price : $1.68 (10Ku)
ARM v7M Architecture

Thumb-2 Instruction Set Architecture
- Mix of 16 and 32 bit instructions for very high code density

Harvard architecture
- Separate I & D buses allow parallel instruction fetching & data storage

Integrated Nested Vectored Interrupt Controller (NVIC) for low latency interrupt processing
- Vector Table is addresses, not instructions
- Designed to be fully programmed in C
- Even reset, interrupts and exceptions

Integrated Bus Matrix
- Bus Arbiter
- Bit Banding – Atomic Bit Manipulation
- Write Buffer
- Memory Interface (I&D) Plus System Interface & Private Peripheral Bus

Integrated System Timer (SysTick) for Real Time OS or other scheduled tasks
• **3-Stage Pipeline**
  – Fetch, Decode & Execute

• **Single Cycle Multiply**

<table>
<thead>
<tr>
<th>Source</th>
<th>Destination</th>
<th>Cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>16b × 16b</td>
<td>32b</td>
<td>1</td>
</tr>
<tr>
<td>32b × 16b</td>
<td>32b</td>
<td>1</td>
</tr>
<tr>
<td>32b × 32b</td>
<td>32b</td>
<td>1</td>
</tr>
<tr>
<td>32b × 32b</td>
<td>64b</td>
<td>3-7*</td>
</tr>
</tbody>
</table>

*UMULL, SMULL, UMLAL, and SMLAL are interruptible and can also complete early depending on source values*

- **Hardware Division**
  - UDIV & SDIV (Unsigned or Signed divide)
  - Instruction takes between 2 & 12 cycles depending on dividend and divisor
  - Closer the dividend and division the faster the instruction completes
  - Instruction is interruptible (abandoned/restarted)
• 2V-3.6V Supply
• 5V tolerant I/Os
• Excellent safe clock modes
• Low-power modes with wake-up
• Internal RC
• Embedded reset
• 36 pins to 100 pins (BGA 5x5, QFN 6x6 available)
• -40/+105°C
Minimální aplikace STM32.

Configuration:

STM32

+3V

Releasing your creativity
Loading / flashing application into STM32

• Loading/flashing application by JTAG

• Loading/flashing application by DFU via USB
Easy-to-Use Tools

Compilers and IDE

Device Programming

IDE and debuggers, GNU compilers
STM32 line of starter kits

- **Choice of complete hardware/software toolsets**
  - Evaluation boards
  - Compilers (Tasking, IAR, ARM or GNU C/C++)
  - Development software (HiTOP3, EWARM, µVision, RIDE)
  - Plus sample code

- **Proven solutions from:**
  - Hitex
  - IAR
  - Keil
  - Raisonance

- **Minimal investment to start developing**
Software Libraries – Speed Time to Market

• **ST software libraries free at www.st.com/mcu**
  
  • C source code for easy implementation of all STM32 peripherals in any application
    
    – **Standard library** – source code for implementation of all standard peripherals. Code implemented in demos for STM32 evaluation board
    
    – **USB software library** – software kit for easy implementation of any USB transfer type. Is already [www.usb.org](http://www.usb.org) certified
    
    – **Motor Control library** – Sensorless Vector Control for 3-phase brushless motors

• **Get the most out of STM32 with an RTOS**

  • Royalty-free, real-time operating systems (RTOS) for embedded applications

  • Wide range of choices from leading RTOS providers
    
    – CMX, FreeRTOS, IAR, Keil, Micrium, Segger
Conclusion

STM32 makes it happen...

- Leading edge 32-bit MCU
  ARM® Cortex™-M3
- Excellent low-power capabilities
- First class peripherals
- Maximum integration
- A wide line of compatible products
- Simple architecture and easy to use tools

... and 32-bit becomes accessible for all!
STM32F10x: product lines

**STM32F10x**

- **Performance Line: STM32F103**
  - CPU: 72MHz
  - Memory: Up to 512KB Flash / 64KB SRAM
  - ADC: 2/3x12-bit (1µs)
  - Temp Sensor
  - USB–FS Device
  - SDIO*
  - I2S*
  - CAN
  - PWM timer

- **USB Access Line: STM32F102**
  - CPU: 48MHz
  - Memory: Up to 128KB Flash / 16KB SRAM
  - ADC: 1x12-bit (1µs)
  - Temp Sensor
  - USB–FS Device

- **Access Line: STM32F101**
  - CPU: 36MHz
  - Memory: Up to 512KB Flash / 48KB SRAM
  - ADC: 1x12-bit (1µs)
  - Temp Sensor

* Only with 256KB, 384KB, or 512KB devices

**All lines include:**

- Multiple communication peripherals
  - Up to 5 x USART, 3xSPI, 2xI²C
- ETM*
- FSMC*
- 2-channel x 12-bit DAC*
- Up to 6 x 16-bit Timers
- Main Osc 4-16MHz
- Internal 8 MHz RC and 40 kHz RC
- Real Time Clock with Battery domain & 32KHz ext osc
- 2 x Watchdogs
- Reset circuitry and Brown Out Warning
- Up to 12 DMA cnls
STM32 connectivity line
STM32F105/107

Both lines include up to:

- 256KB FLASH
- Multiple communication peripherals: USART, SPI, I2C
- Multiple 16-bit TIMERS
- Dual DAC
- ETM
- Main Osc 3-16MHz
- Internal 8 MHz RC and 40 kHz RC
- Real Time Clock
- 2 x Watchdogs
- Reset circuitry
- 2 x 12-bit ADC 1µs
- Temp sensor
- PWM Timer
- Up to 12 channels DMA
- 80% GPIO ratio

Pin to Pin Compatible with Existing Devices

Samples: June 09

STM32F107

- 72MHz CPU
- Up to 64KB SRAM
- USB 2.0 OTG FS
- 2x CAN 2.0B
- 2x I2S High Quality Audio
- Ethernet IEEE1588

STM32F105

- 72MHz CPU
- Up to 64KB SRAM
- USB 2.0 OTG FS
- 2x CAN 2.0B
- 2x I2S High Quality Audio
STM32F10x High-density Series Block Diagram

- ARM 32-bit Cortex-M3 CPU
- Nested Vectored Interrupt Controller (NVIC) w/ 60 maskable IT + 16 prog. priority levels
- Embedded Memories:
  - FLASH: up to 512kB
  - SRAM: up to 64kB
- External memory interface FSMC: support NAND, SRAM, NOR, PC Cards and others memory devices
- 2 x DMA w/ 12 channels
- SDIO: support SD, SDIO, MMC and CE-ATA cards
- Power Supply with internal regulator and low power modes:
  - 2V to 3.6V supply
  - 4 Low Power Modes with Auto Wake-up
- Integrated Power On Reset (POR) / Power Down Reset (PDR) + Programmable voltage detector (PVD)
- Backup domain w/ 84B user data
- Up to 72 MHz frequency managed & monitored by the Clock Control w/ Clock Security System
- Rich set of peripherals & I/Os
  - Embedded low power RTC with \( V_{BAT} \) capability
  - Dual Watchdog Architecture
  - 9 Timers w/ advanced control features (including Cortex SysTick)
  - 12 communications Interfaces
  - Up to 112 I/Os (144 pin package) w/ 16 external interrupts/event
  - Up to 3x12-bits 1Msps ADC w/ up to 21 channels and Embedded temperature sensor w/ +/-1.5° linearity with \( T^\circ \)
  - 12-bits DAC w/ 2 channels
Memory Mapping and Boot Modes

**Addressable memory space of 4 GBytes**
- RAM: up to 64 kBytes
- FLASH: up to 512 kBytes

**Boot modes**
Depending on the Boot configuration, Embedded Flash Memory, System Memory or Embedded SRAM Memory is aliased at @0x00

<table>
<thead>
<tr>
<th>BOOT Mode Selection Pins</th>
<th>Boot Mode</th>
<th>Aliasing</th>
</tr>
</thead>
<tbody>
<tr>
<td>BOOT1</td>
<td>BOOT0</td>
<td></td>
</tr>
<tr>
<td>x</td>
<td>0</td>
<td>User Flash</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>System Memory</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Embedded SRAM</td>
</tr>
</tbody>
</table>

**System Memory:** contains the Bootloader used to re-program the FLASH through USART1.
For more details refer to AN2606 & UM0462
A PC Windows Demonstrator is available as well.

**Boot from Embedded SRAM**:
In the application initialization code you have to Relocate the Vector Table in SRAM using the NVIC Exception Table and Offset register.
System Architecture

- **Multiply possibilities of bus accesses to SRAM, Flash, Peripherals, DMA**
  - BusMatrix added to Harvard architecture allows parallel access

- **Efficient DMA and Rapid data flow**
  - Direct path to SRAM through arbiter, guarantees alternating access
  - Harvard architecture + BusMatrix allows Flash execution in parallel with DMA transfer

- **Increase Peripherals Speed for better performance**
  - Dual Advanced Peripheral buses (APB) architecture w/ High Speed APB (APB2) up to 72MHz and Low Speed APB (APB1) up to 36MHz
  - Allows to optimize use of peripherals (18MHz SPI, 4.5Mbps USART, 72MHz PWM Timer, 18MHz toggling I/Os)

Buses are not overloaded with data movement tasks.
STM32F10x: Low Power

Low Voltage 2.0V to 3.6V operation

0.5mA/ MHz in RUN mode from Flash

**Startup time** From STOP (Vreg Off) **7µs**
**Startup time** From STOP (Vreg On) **4µs**
**Startup time** From STANDBY **40µs**

STOP
- All clocks off, Reset ON, RAM ON
  (registers’ content preserved)

STANDBY
- All clocks off, Reset ON, RAM OFF but
  20 bytes available for backup
Reset + Clock

&

GPIO
Reset and Clock Control (RCC)
**RESET Sources**

**System RESET**
- Resets all registers except some RCC registers and BKP domain
- **Sources**
  - Low level on the NRST pin (External Reset)
  - WWDG end of count condition
  - IWDG end of count condition
  - A software reset (through NVIC)
  - Low power management Reset

**Power RESET**
- Resets all registers except BKP domain
- **Sources**
  - Power On/Power down Reset (POR/PDR)
  - When exiting STANDBY mode

**Backup domain RESET**
- Resets all BKP domain
- **Sources**
  - Setting BDRST bit in RCC BDCR register
  - VDD or VBAT power on, if both supplies have previously been powered off.
On Chip Oscillators

- Multiple clock sources for full flexibility in RUN/Low Power modes
  - **HSE** (High Speed External oscillator): 4MHz to 16MHz main osc which can be multiplied by the PLL to provide a wide range of frequencies
  - **HSI** (High Speed Internal RC): factory trimmed internal RC oscillator 8MHz +/- 1% over 0-70°C temp range
    - Feeds System clock after reset or exit from STOP mode for fast startup (startup time: 2us max)
    - Backup clock in case HSE osc is failing
    - **Note:** When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 64 MHz.
  - **LSI** (Low Speed Internal RC): 40KHz internal RC for IWDG and optionally for the RTC used for Auto Wake-Up (AWU) from STOP/STANDBY mode
  - **LSE** (Low Speed External oscillator): 32.768kHz osc provides a precise time base with very low power consumption (max 1µA). Optionally drives the RTC for Auto Wake-Up (AWU) from STOP/STANDBY mode.
Clock Scheme

STM32

- HSI RC
- HSE Osc
- LSE Osc
- LSI RC
- SYSCLK
- PLLCLK
- OSC\_OUT
- OSC\_IN
- OSC32\_IN
- OSC32\_OUT
- 4-16 MHz
- 8MHz
- 32.768KHz
- 3.28KHz
- 40KHz
- 128
- 2
- 2
- x2...x16
- Up to 72 MHz
- Up to 72 MHz
General Purpose and Alternate Function
I/O (GPIO and AFI0)
**GPIO Features**

- Up to 80 multifunction bi-directional I/O ports available: 80% IO ratio
  - Standard I/Os 5V tolerant
  - The GPIOs can sink 25mA (total currents sunk is 150mA)
  - 18 MHz Toggling
  - Configurable Output Speed up to 50 MHz
  - Up to 16 Analog Inputs
  - Alternate Functions pins (like USARTx, TIMx, I2Cx, SPIx, CAN, USB...)
  - Up to 80 GPIOs can be set-up as external interrupt (up to 16 lines at time)
  - One I/O can be used as Wake-Up from STANDBY (PA.00)
  - One I/O can be set-up as Tamper Pin (PC.13)
  - All Standard I/Os are shared in 5 ports (GPIOA..GPIOE)
  - Atomic Bit Set and Bit Reset using BSRR and BRR registers
  - Locking mechanism to avoid spurious write in the IO registers
    - When the LOCK sequence has been applied on a port bit, it is no longer possible to modify the configuration of the port bit until the next reset (no write access to the CRL and CRH registers corresponding bit).
GPI O Configuration Modes

<table>
<thead>
<tr>
<th>Configuration Mode</th>
<th>CNF1</th>
<th>CNF0</th>
<th>MOD1</th>
<th>MOD0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Input</td>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Floating (Reset State)</td>
<td>0</td>
<td>1</td>
<td></td>
<td>00</td>
</tr>
<tr>
<td>Input Pull-Up</td>
<td>1</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Pull-Down</td>
<td>1</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Push-Pull</td>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Open-Drain</td>
<td>0</td>
<td>1</td>
<td>01: 10 MHz</td>
<td>10: 2 MHz</td>
</tr>
<tr>
<td>AF Push-Pull</td>
<td>1</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AF Open-Drain</td>
<td>1</td>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) VDD for standard I/Os and VDD_FT is a potential specific to five-volt tolerant I/Os and different from VDD.
AFIO Features

- Event Out signal generation
  - **Pulse** generation with SEV instruction: to wake-up an other MCU from low power mode through its Event In signal
  - Each IO can be used as Event Out

- GPIO Software Remapping
  - Some Alternate function can be remapped in two different pins allowing **optimization** of the pin out
  - All SWJ-DP I/O pins can be used as GPIO

- EXTI Lines Configuration
  - Each EXTI line is shared with **all GPIO** ports: EXTI Linexx → GPIO[A..E].xx
External Interrupt/ Event Controller (EXTI)
EXTI Features

- Up to 19 Interrupt/Events requests
  - Up to 80 GPIOs can be used as EXTI line(0..15)
  - EXTI line 16 connected to PVD output
  - EXTI line 17 connected to RTC Alarm event
  - EXTI line 18 connected to USB Wake-up from suspend event

- Two Configuration mode:
  - **Interrupt** mode: generate interrupts with external lines edges
  - **Event** mode: generate pulse to wake-up system from SLEEP and STOP modes

- Independent trigger (rising, falling, rising & falling) and mask on each interrupt/event line

- Dedicated status bit for each interrupt line
ADC & DAC

STM32 presentation ČVUT version 1.0

Luděk Holoubek

STM32 presentation ČVUT version 1.0

Luděk Holoubek
Analog-to-Digital Converter (ADC)
ADC Features (1/2)

- **ADC conversion rate**: 1 MHz and 12-bit resolution
  - 1μs conversion time at 56 MHz
  - 1.17μs conversion time at 72 MHz
- **Conversion range**: 0 to 3.6 V
- **ADC supply requirement**: 2.4V to 3.6 V
- **ADC input range**: VREF- ≤ VIN ≤ VREF+ (VREF+ and VREF- available only in LQFP100 package)
- **Dual mode** (on devices with 2 ADCs): 8 conversion mode
- **Up to 18 multiplexed channels**:
  - 16 external channels
  - 2 internal channels: connected to Temperature sensor and internal reference voltage (VREFINT = 1.2V)
ADC conversion modes

Four conversion modes are available:

- Single channel single conversion mode
- Multi-channels (Scan) single conversion mode
- Single channel continuous conversion mode
- Multi-channels (Scan) continuous conversion mode
**ADC Features (2/2)**

- **Sequencer**-based scan mode for up to 16 conversion
- External **trigger** option for both regular and injected conversion
- Channel by channel programmable **sampling** time
- **Discontinuous** mode on regular and injected groups
- Left or right Data alignment with inbuilt data coherency
- Analog **Watchdog** on high and low thresholds
- **Interrupt** generation on:
  - End of Conversion
  - End of Injected conversion
  - Analog watchdog
- **DMA** capability (only on ADC1)
ADC Analog Watchdogs

- 12-bit programmable analog watchdog **low** and **high** thresholds
- Enabled on one, or all converted channels: one regular or/and injected channel, all injected or/and regular channels.
- **Interrupt** generation on low or high thresholds detection
DMA

- DMA available only on ADC1
- DMA request generated on each ADC1 end of regular channel conversion (Not in injected channels)

**Example:** - Conversion of regular channels: 0, 1, 2, 3, 4, 5, 6, 7 and 8
- Convert data stored in ConvertedValue_Tab[9]
- DMA transfer enabled (destination address auto incremented)

**Note:** EOC flag cleared at end of regular channels conversion due to DMA access to ADC1 DR register
Digital-to-Analog Converter (DAC)
DAC Features

- **Two** DAC converters: **one** output channel for each one
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave or Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- DAC supply requirement: 2.4V to 3.6 V
- Conversion range: 0 to 3.6 V
- DAC outputs range: $0 \leq \text{DAC\_OUT}_x \leq \text{VREF}^+$ (VREF+ and VREF- available only in 100 and 144 pins package)
  - ADC and DAC share the same VREF+
Timers
Advanced Control And General Purpose Timers
Counter Modes

There are three counter modes:

- **Up counting mode**
- **Down counting mode**
- **Center-aligned mode**

When using the Repetition Counter (case of TIM1 only)

![Graph showing Center Aligned, Up counting, and Down counting modes with RCR = 0 and RCR = 2.](image)
PWM Mode

The PWM mode allows to **generate**:
- 7 independent signals for TIM1
- 4 independent signals for TIM2, 3 and 4
- The frequency and a duty cycle determined as follow:
  - One **auto-reload** register to defined the PWM period.
  - Each PWM channel has a **capture compare** register to define the duty cycle.

**Example:** to generate a 40 KHz PWM signal w/ duty cycle of 50% on TIM1 clock at 72MHz:
- Load Prescaler register with 0 (counter clocked by TIM1CLK/(0+1)), Auto Reload register with 1799 and CCRx register with 899

There are two configurable PWM modes:
- Edge-aligned Mode
- Center-aligned Mode

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**Edge-aligned Mode**

**Center-aligned Mode**
Communication
LCD modules interface signals

LCD /RD: The ready signal indicates to the 8080 that valid memory or input data is available on the 8080 data bus.

LCD /WR: The /WR signal is used for memory write or I/O output control. The data on the data bus is stable while the /WR is active low (/WR = 0).

LCD RS: RAM Data/ Register Data Selection

LCD /CS: Chip Select

LCD D[0:15]: Bidirectional data bus

All LCD Signals are controlled by FSMC

Application Note is available from www.st.com/mcu

AN2790: TFT LCD interfacing with the High-density STM32F10xxx FSMC
NAND/ PCCARD interface signals

The FSMC generates the appropriate **signal to drive** the following types of memories:

- PC Card, CompactFlash, CF+ or PCMCIA
- NAND Flash
  - 8-bit
  - 16-bit

![Diagram of NAND/PC Card Memory Controller with signals](image)

- **Shared Signals**
  - FSMC_A[25:0]
  - FSMC_D[15:0]
  - FSMC_NOE
  - FSMC_NWE
  - FSMC_NWAIT

- **NAND Signals**
  - FSMC_NCE[3:2]
  - FSMC_INT[3:2]

- **PC CARD Signals**
  - FSMC_INT
  - FSMC_NCE4_1
  - FSMC_NCE4_2
  - FSMC_NIORD
  - FSMC_NIOWR
  - FSMC_NIOS16
  - FSMC_NREG
  - FSMC_CD
SDIO interface
SDIO Features (1/2)

- Full compliance with
  - **MMC** - Multimedia Card System Specification Version 4.2. Card support for three different data bus modes: 1-bit (default), 4-bit and 8-bit
  - Full compatibility with previous versions of Multimedia Cards (forward compatibility)

- **SD** Memory Card Specifications Version 2.0
- **SD I/O** Card Specification Version 2.0: card support for two different data bus modes: 1-bit (default) and 4-bit

- Full support of the **CE-ATA** features (full compliance with CE-ATA digital protocol Rev1.1)
- Data transfer up to 48 MHz
SD/SDIO & MMC Cards

- The SDIO has **10 pins** to control different kinds of memory cards.
- Only 6 pins (SDIO_CMD, SDIO_CK, SDIO_D[3:0]) at most for **SD** cards (SD full size, miniSD, microSD).
- Only 6 pins (SDIO_CMD, SDIO_CK, SDIO_D[3:0]) at most for **SDIO** cards (SD full size, miniSD, microSD).
- **10 pins** (SDIO_CMD, SDIO_CK, SDIO_D[7:0]) at most for **MMC** cards (MMC full size, RS-MMC, MMC+, and MMCMobile).
CE-ATA Devices
Serial Peripheral Interface (SPI)
Full Duplex Communication

- SPI supports Full duplex and Tx-Only communication mode:
  - Performance: speed up to 18MHz
  - Full-duplex, three-wire synchronous transfer

![Diagram showing Full Duplex Communication](image)
SPI SD/ MMC Card Support

- Basic SD/MMC support (SPI protocol):
  - Performance: speed up to 18MHz
  - Error checking: hardware CRC calculation
I2S mode
I2S supports only simplex communication mode:
- Simplex, three-wire synchronous audio transfer

- The master and slave configuration is managed only by software. The master device is the CK and WS generator.
- The master/slave modes and transmit/receive directions can be switched dynamically by software.

**Optional feature activated by software**

* Depends on the Codec control method
Inter Integrated Circuit (I2C)
**I2C Features (1/2)**

- **Multi** Master and slave capability – BUS!!!
- **Controls all** I²C bus specific sequencing, protocol, arbitration and timing
- Standard and fast I²C mode (up to 400kHz)
- 7-bit and 10-bit **addressing** modes
- SMBus 2.0 Compatibility
- PMBus Compatibility

- Configurable PEC (Packet Error Checking) Generation or Verification:
  - PEC value can be transmitted as last byte in Tx mode
  - PEC error checking for last received byte
I2C supports dual addressing capability to acknowledge 2 slave addresses.
Universal Synchronous Asynchronous Receiver Transmitter (USART)
**USART Features (1/2)**

- **Three** USART: USART1 High speed APB2 and USART2,3 on Low speed APB1
- **Data** can be 8 or 9 bits
- Even, odd or no-**parity** bit generation and detection
- 0.5, 1, 1.5 or 2 **stop bit** generation
- Programmable **baud rate** generator
  - Integer part (12 bits)
  - Fractional part (4 bits)
- Support hardware **flow control** (CTS and RTS)
- Dedicated transmission and reception **flags** (TxE and RxNE) with interrupt capability
- Support for **DMA**
  - Receive DMA request
  - Transmit DMA request

Up to 4.5 Mbps
**Synchronous Mode**

-USART supports Full duplex synchronous communication mode
  - Full-duplex, three-wire synchronous transfer
  - USART Master mode only
  - Programmable clock polarity (CPOL) and phase (CPHA)
  - Programmable Last Bit Clock generation
  - Transmitter Clock output (SCLK)

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**Full Duplex**

[Diagram showing full-duplex communication between Master and Slave with pins SCK, MISO, MOSI, NSS, and clock line SCLK]
IrDA SIR Encoder Decoder

- USART supports the IrDA Specifications
  - Half-duplex, NRZ modulation,
  - Max bit rate 115200 bps
  - 3/16 bit duration for normal mode
Smart Card mode

- USART supports Smart Card Emulation ISO 7816-3
  - Half-Duplex, Clock Output (SCLK)
  - 9Bits data, 0.5 Stop Bit in receive, 1.5 Stop Bits in transmit
  - Parity Error Generation with NACK transmission
  - Programmable Guard Time (data processing)
  - Programmable Clock Prescaler to guarantee a wide range clock input
**Single Wire Half Duplex mode**

- USART supports Half duplex synchronous communication mode
- Only Tx pin is used (Rx is no longer used)
- Used to follow a single wire Half duplex protocol.
Universal Serial Bus interface (USB Device)
USB Features

- **Full** speed USB 2.0 transfer.
- **USB OTG** in the latest version of the STM32F107...
STM32F10x USB Developer kit

STM32F10x USB Library
- USB 2.0 full speed certified
- All in Strict ANSI-C
- Independent from any SW tool chain
- Independent from the Firmware library
- Self documented

STM32F10x USB Developer Kit demos
- Cover all USB transfer types
- Independent from any SW tool chain
- Running on STMicroelectronics STM32F10x-EVAL board and can be easily tailored to any other hardware
LED dimming - Evaluation board – STM32
LED dimming - Evaluation board – STM32

STM32

USB

ESD for USB

USBUF01P6

SPI

LED driver

STP24DP05

SPI

LED driver

STP24DP05

LEDs

Power supply

ST1S10

STM32

4.5V

STM32

3.3V

USB

LED Drivers

Open jumpers

7-18V

Short jumpers

JTAG

RGB LEDs

POWER

Buttons

Error Flag

Temperature flag

RESET

Knob
Questions?

- Diplomky
- Předměty s STM32
- Vzorky STM32
- Materiály
- ...

STM32 presentation ČVUT version 1.0
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Thank You!