FET (Field Effect Transistor)

Few important advantages of FET over BJT Transistors
1. Unipolar device - operation depends on only one type of charge carriers (h or e)
2. Voltage controlled Device (gate voltage controls drain current)
3. Very high input impedance (≈10^9-10^12 Ω)
4. Source and drain are interchangeable in most Low-frequency applications
5. Low Voltage Low Current Operation is possible (Low-power consumption)
6. Less Noisy as Compared to BJT
7. No minority carrier storage (Turn off is faster)
8. Self limiting device
9. Very small in size, occupies very small space in ICs
10. Low voltage low current operation is possible in MOSFETS

JFET – Junction Field Effect Transistor

- The JFET transistor has the control electrode of opposite semiconductor conductivity than the channel
- The PN junction is reverse polarized.
- Voltage on the gate modulates the OPN (space charge), thereby control the thickness of the channel and hence channel conductivity

JFET Operation

Real JFET construction

- JFET Cross-section
Operation principle

When $V_{DS}$ is small

When $V_{GS}$ is zero

Output or Drain ($V_D$-$I_D$) Characteristics of $n$-JFET

Non-saturation (Ohmic) Region:

The drain current is given by

$$I_D = \frac{2}{3} \left( \frac{V_{GS} - V_P}{P} \right)$$

Saturation (or Pinchoff) Region:

$$I_D = \frac{2}{3} \left[ \left( \frac{V_{GS} - V_P}{V_D} \right)^2 \right]$$

$$I_{DSS} = \frac{V_{GS} - V_P}{P}$$

Where, $I_{DSS}$ is the short circuit drain current, $V_P$ is the pinch off voltage.

Limiting parameters of JFET

- Breakdown voltage $V_{DS}$
- Maximal power dissipation $P_{D_{max}}$
- Maximal Gate current $I_G$

Basic circuits with JFET

Current sources

N-JFET for $V_{DS} = 10V$
Basic circuits with JFET

- Setting of operational point for class A

JFET as small signal amplifier

- Common source amplifier:

MESFET Transistor

- PN junction (G-S) is made by Schottky diode
- Typical components on GaAs
- Applications: High frequency amplifiers, switches, etc.

MOSFET Transistor

- Transistor is driven by electric field
- Transistor structure Metal M – Oxide O – Semiconductor S
- Metal is now mainly replaced PolySi, Oxide SiO₂
- Very high entrance gate resistance, up to $10^{14}$
- Transistor can be very small ~ 32 nm
- Very huge integration density ~ 1 000 000 000 components on chip
- Very small static power consumption
- Enhanced mode transistor (conduction channel exists when $V_{GS} = 0$.)

NMOS transistor structure

PMOS transistor structure
MOS capacitor - no contact

Bend diagrams:

\[ \text{metal} \]

\[ \text{P} \quad \text{N}_x \]

\[ \text{oxide} \]

\[ \text{E}_{\text{ox}} \]

\[ \text{eV}_{\text{bi}} \]

\[ \text{eV} \]

\[ \text{E}_{\text{vac}} \]

\[ \text{E}_s \]

\[ \text{E}_c \]

\[ \text{E}_F \]

\[ \text{E}_i \]

MOS capacitor - no gate voltage and no bias

\[ \text{metal} \quad \text{oxide} \quad \text{N}_x \]

\[ \text{V}_{\text{G}} = \text{V}_{\text{bi}} + \text{V}_{\text{G}} \]

\[ \text{p}_p \text{n}_p = \text{n}_i^2 \]

Depletion mode

\[ \text{V}_{\text{G}} \approx \text{V}_{\text{B}} \]

\[ \text{V}_{\text{B}} < \text{V}_{\text{s}} < 2 \text{V}_{\text{B}} \]

Inversion layer formation – conduction channel

\[ \text{N}^+ \quad \text{N}^+ \]

Depletion region

\[ \text{Holes} \]

MOS capacitor + gate voltage and no bias

\[ \text{metal} \quad \text{oxide} \quad \text{N}_x \]

\[ \text{V}_{\text{G}} = \text{V}_{\text{bi}} + \text{V}_{\text{G}} \]

\[ \text{Depletion mode} \]

\[ \text{V}_{\text{G}} \approx \text{V}_{\text{B}} \]

\[ \text{V}_{\text{B}} < \text{V}_{\text{s}} < 2 \text{V}_{\text{B}} \]

MOS capacitor + gate voltage and no bias

\[ \text{metal} \quad \text{oxide} \quad \text{N}_x \]

\[ \text{V}_{\text{G}} = \text{V}_{\text{bi}} + \text{V}_{\text{G}} \]

\[ \text{Depletion layer} \]

\[ \text{Inversion layer} \]

\[ \text{V}_{\text{G}} \approx \text{V}_{\text{B}} \]

\[ \text{V}_{\text{B}} < \text{V}_{\text{s}} < 2 \text{V}_{\text{B}} \]

MOS capacitor in inversion mode – fields and charges

\[ \text{metal} \quad \text{oxide} \quad \text{N}_x \]

\[ \text{V}_{\text{G}} = \text{V}_{\text{bi}} + \text{V}_{\text{G}} \]

\[ \text{Depletion mode} \]

\[ \text{V}_{\text{G}} \approx \text{V}_{\text{B}} \]

\[ \text{V}_{\text{B}} < \text{V}_{\text{s}} < 2 \text{V}_{\text{B}} \]
MOS capacitor-deep inversion

Mobile inversion charge

MOS capacitor in deep inversion mode – fields and charges

Inversion layer formation – conduction channel

When \( V_{DS} \) is applied

Triode region: \( (V_{GS} > V_t, V_{DS} < V_{GS} - V_t) \)

Drain Current:

\[
I_D = \mu \frac{W}{L} \cdot \frac{V_{GS} - V_t}{2} \cdot \left( V_{DS} - \frac{V_{GS} - V_t}{2} \right)
\]
**Active region: (VGS>Vt, VDS·VGS·Vt)**

- **Drain Current:**
  \[ I_D = \mu C_{ox} \left( \frac{W}{L} \right) (V_{GS} - V_t) \]

- **Channel length modulation parameter:**
  \[ L' = L - \Delta L \]
  \[ \frac{\Delta L}{L} = 2V_{DS} \]

- **Output resistivity:**
  \[ r_o = \frac{1}{2L} \]

- **Body (bulk) transconductance:**
  \[ g_m = \frac{\gamma}{2 \sqrt{V_{DS} + 2\Phi}} \]
  \[ \frac{g_m}{g_m} = \chi \]
  (typical 0.1 - 0.3)

- **Transconductance:**
  \[ g_m = \mu C_{ox} \left( \frac{W}{L} \right) (V_{GS} - V_t) \]

- **Transition frequency:**
  \[ f_T = \frac{g_m}{2\pi(C_{ox} + C_{Gd} + C_{Gg})} \]