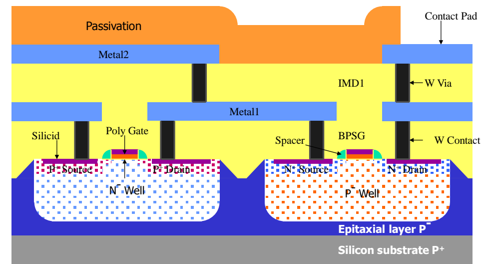
# CMOS Technology
## Step by step

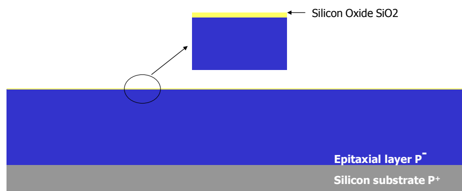
11. Lecture

## CMOS cross-section



## CMOS technology - Local oxidation

Growth of thermal oxide: A very thin layer of $SiO_2$ (~ 200A) reduces the mechanical stress between the silicon and the future silicon nitride layer.



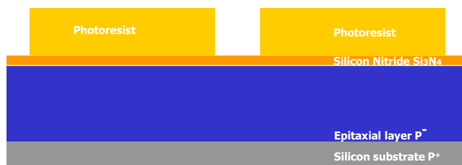
## Building of insulation trenches

Silicon Nitride deposition: A layer of silicon nitride (Si3N4) (~ 2500A) is applied by CVD (Chemical Vapor Deposition). Main purpose of this layer is to prevent oxidation of isolation trenches outside.

## Building of insulation trenches

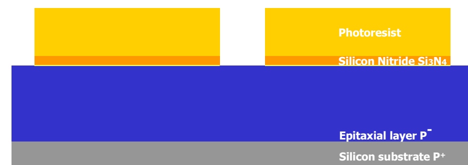
**ACTIVE AREA mask** – Photoresist Application:

0.5 - 1.0 thick layer



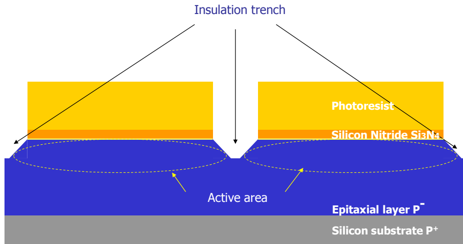
## Building of insulation trenches

Nitride and oxide etching: Reactive ion etching (RIE)



## Building of insulation trenches

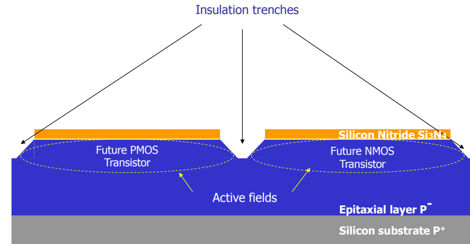
Etching of trenches in silicon: RIE - This step defines the active area, where the transistors will be placed






## Building of insulation trenches

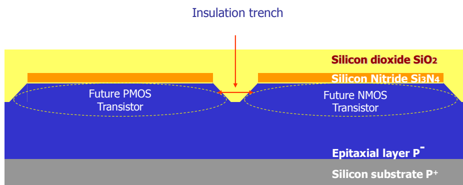
Removal of photoresist:






## Building of insulation trenches

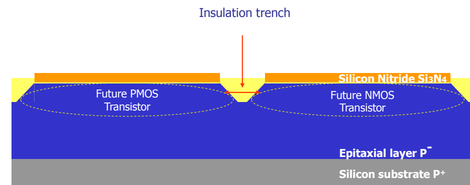
The growth of insulating oxide: using local oxidation or CVD method. Silicon oxide acts as insulation between transistors.






## Building of insulation trenches

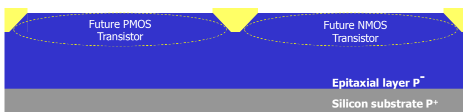
Removal of Silicon dioxide: Silicon dioxide is removed from the surface by Chemical Mechanical Polishing (CMP). CMP stops within nitride layer.






## Building of insulation trenches

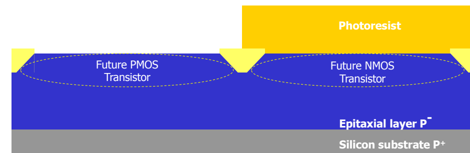
Removal of silicon nitride: Using wet etching method in H3PO4. Isolation trenches are done (Shallow Trench Isolation - STI)





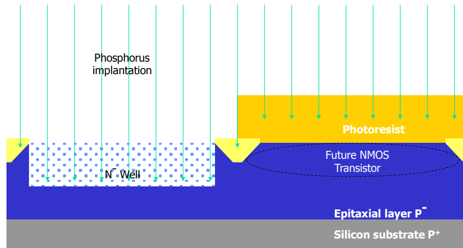

## N- well formation

**N-Well Mask** : Application of strong photoresist, which prevents implantation of impurities into unwanted places.



## N- well formation

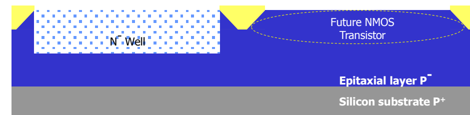
N- well ion implantation : Phosphorus atoms are accelerated by high electromagnetic field energy. An N-well for future PMOS transistor is created.






## N- well formation

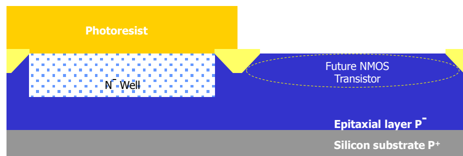
Photoresist removal:






## P- well formation

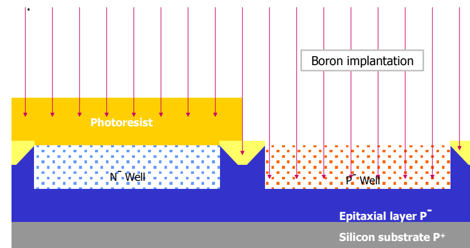
**P-Well Mask**: Application of photoresist for the P- well formation






## P- well formation

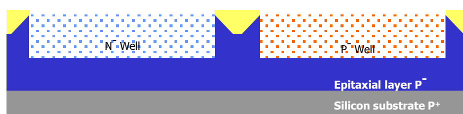
Ion Implantation of P- well: Boron is accelerated by high electromagnetic field energy. An P-well for future NMOS transistor is created.






## P- well formation

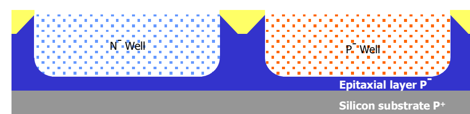
Photoresist removal





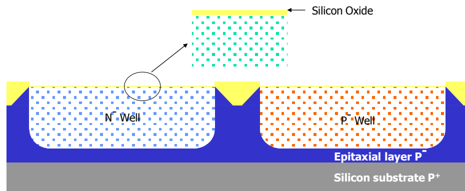

## P- and N- well Annealing

Impurities Annealing : This high temperature process step starts diffusion and removes defects in single crystal which is caused by ion implantation.



## Silicon oxide formation removes defects from silicon surface

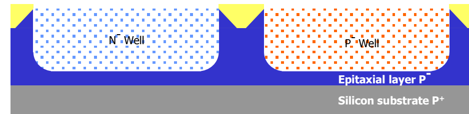
Growth of silicon dioxide : Thermal growth of thin layer (~ 250 A). Silicon dioxide eliminates defects from the surface prior to gate oxide deposition






## Silicon oxide removal

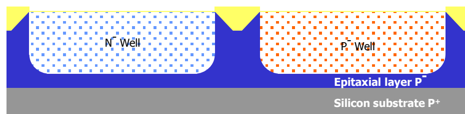
Removal od „sacrificed“ oxide: Silicon dioxide is removed by wet etching. After this operation, the substrate surface is perfectly clean and flat.






## Gate oxide forming

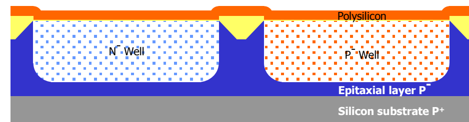
Gate oxide forming: **This is one of the most critical technological process!** A very thin layer (10-100A) forms the gate dielectrics for both transistors. Silicon dioxide must be extremely clean, and its thickness can vary + / - 1A.






## Gate forming

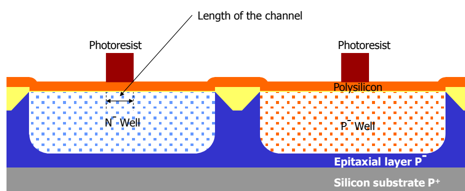
Deposition of Polysilicon: Polycrystalline silicon is applied by CVD 1500-3000 A.






## Gate Forming

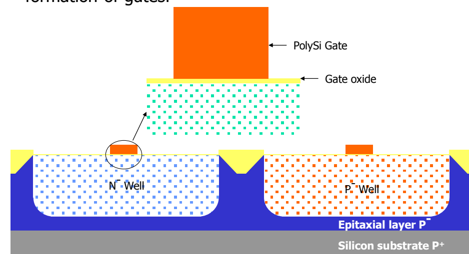
**POLYSI Mask** : Defines the gates of both transistors. **Along with the gate oxide this is the most critical technological step!** Defines the size of the channel length of transistors.





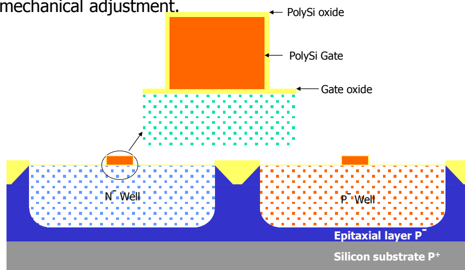

## Gate forming

Etching of Polysilicon and photoresist removal : The RIE (Reactive Ion Etching) method . This is the complete formation of gates.



## Gate forming

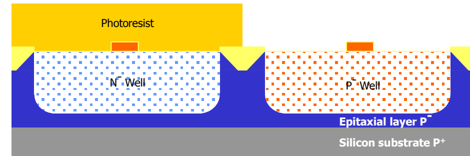
Oxidation of polysilicon: A thin layer of oxide is used to separate gates and subsequent nitride layer. Important for mechanical adjustment.






## Formation of diffusion fields for source and drain

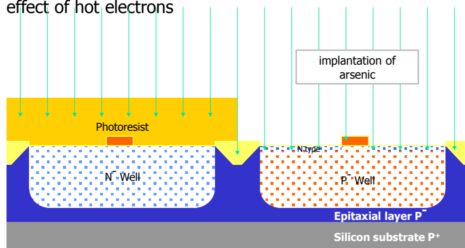
**N-diff Mask**: Masking ion implantation for the N area






## Source and Drain fields formation

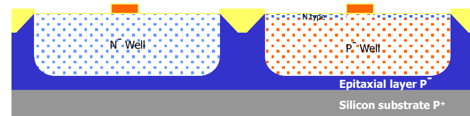
Ion Implantation for NMOS Transistor: Very shallow (low energy) ion implantation of arsenic ions. This step forms the tip of the LDD (Lightly Doped Drain) structure. LDD Reduces the effect of hot electrons






## Source and Drain fields formation

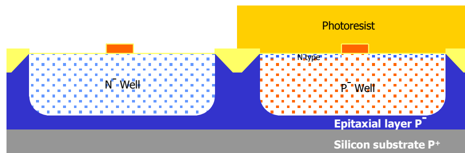
Photoresist removal:






## Source and Drain fields formation

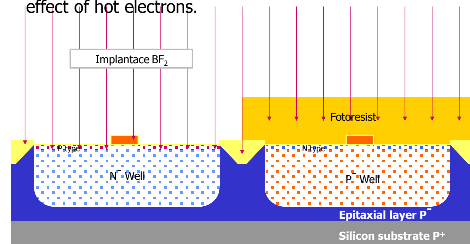
**P-diff Mask**: Mask for the P+ field for Source and Drain of PMOS tranzistor





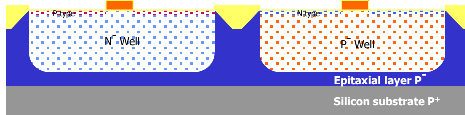

## Source and Drain fields formation

Ion Implantation for PMOS Transistor: Very shallow (low energy) BF2 implantation. This step forms the tip of the LDD (Lightly Dopped Drain) structure. Reduces the effect of hot electrons.



## Source and Drain fields formation

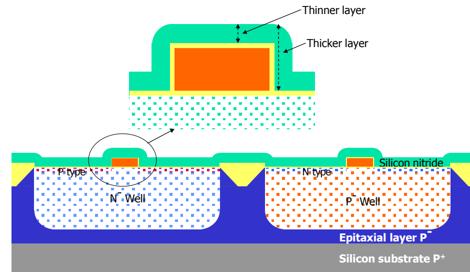
Photoresist removal






## Source and Drain fields formation

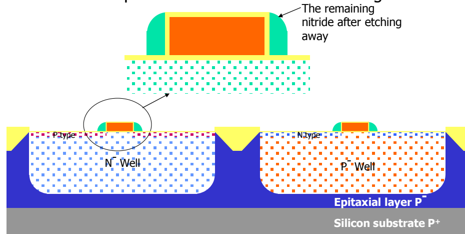
Deposition of Silicon Nitride: CVD 1200-1800A. For LDD structure masking






## Source and Drain fields formation

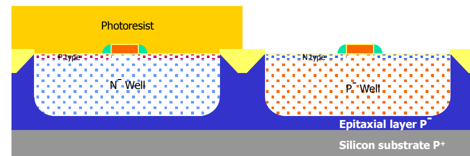
Nitride Etching - formation of side walls for LDD masking : Using RIE nitride is etched vertically on its thickness, so after etching the side walls remain. They acts as a mask for the ion implantation of source and drain regions.






## Source and Drain fields formation

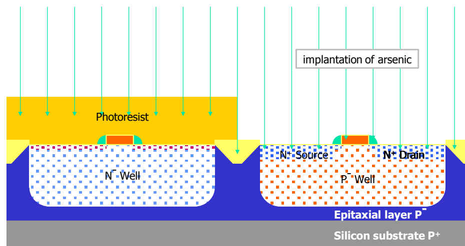
**N-diff Mask**: Masking for ion implantation of N






## Source and Drain fields formation

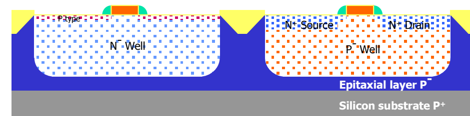
Ion implantation for NMOS Transistor: Deeper (High energy) ion implantation usually arsenic. A large dose. This step forms the LDD (Lightly Dopped Drain) structure, which reduces the effect of hot electrons.





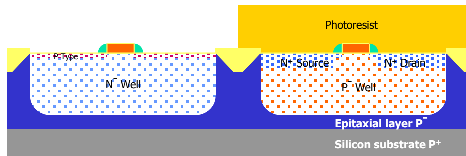

## Source and Drain fields formation

Photoresist removal:



## Source and Drain fields formation

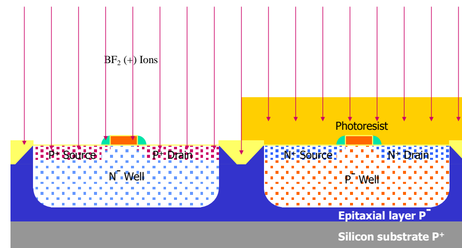
**P-diff Mask**: Masking for ion implantation of P area






## Source and Drain fields formation

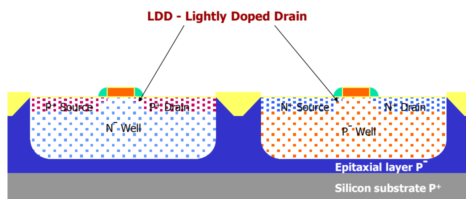
Ion implantation for NMOS Transistor: Deeper (High energy) ion implantation most BF2. A large dose. This step forms the LDD (Lightly Dopped Drain) structure, which reduces the effect of hot electrons.






## Source and Drain fields formation

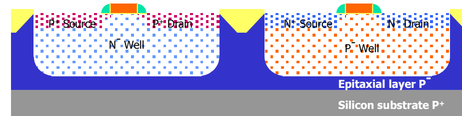
Removal of photoresist and diffusing of impurities: This step completes all electronic component process on a chip. It remains to create interconnecting metallization.






## Silicon oxide removal

Silicon oxide removal:

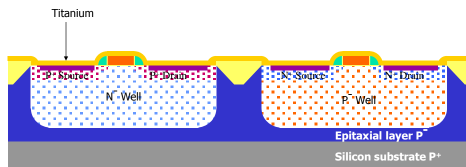





## Forming of Silicide

Deposition of Titanium: A thin layer (200-400A) is applied to the entire surface of the substrate

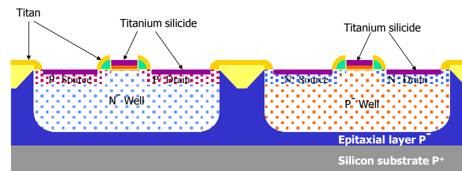
Silicide form properties of metal-semiconductor interface and especially avoid diffusing of metal atoms into semiconductor active area





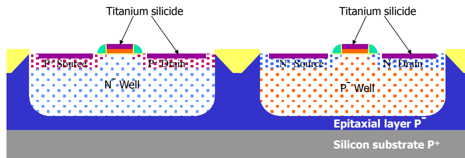

## Forming of Silicide

Forming of Titanium silicide: Rapid thermal heating (800 C°) in Nitrogen starts the reaction of titanium and silicon. This will provide a Titanium sillicide. In other areas, remains the original layer of Titan unchanged. This technological step creates a so-called Self-Aligned Silicide



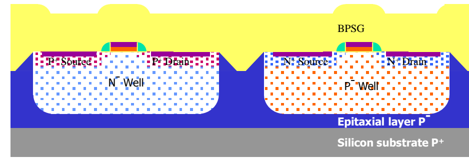
## Forming of Silicide

Removal of Titanium: Using wet etching $NH_4OH + H_2O_2$. $TiSi_2$ silicide remains to form ohmic contact between the silicon and the metallization



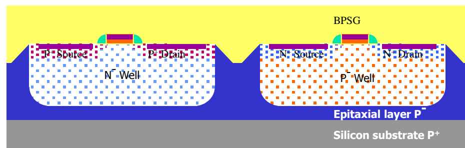
## First metallization layer

Deposition of BPSG: Silicon oxide doped with a small amount of boron and phosphorus. Deposition by CVD. The approximate thickness is 1 micrometre. This layer creates electrical insulation between the active components and the first metallization layer.



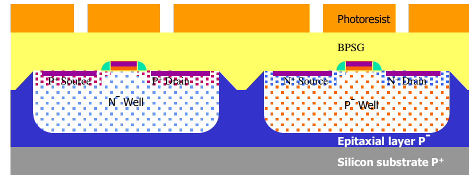
## First metallization layer

Polishing BPSG: Chemical-Mechanical Polishing (CMP) forms flat and smooth surface of the BPSG layer.



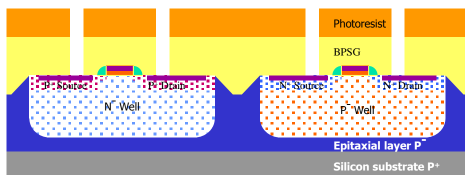
## First metallization layer

**Mask of Contacts**: Application of photoresist, lithography mask according to contacts. Etching of the holes in the BPSG layer to allow electrical connection of components. Challenging technological step.



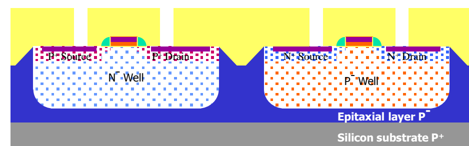
## First metallization layer

Etching of contacts: RIE.



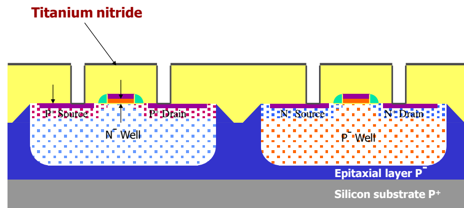
## First metallization layer

Photoresist removal:



## First metallization layer

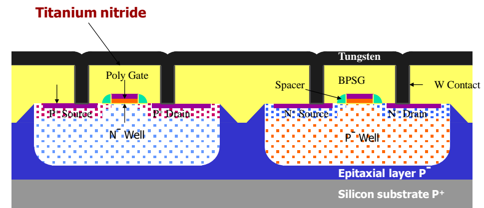
Deposition of Titanium Nitride: TiN through a vapour film thickness of 200A. Layer serves to perfect adhesion to the metallization layer of insulation






## First metallization layer

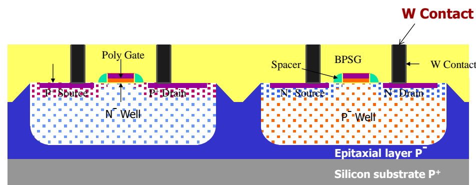
Tungsten Depositon : By this method, the conformal layer of metal is taken up (by CVD) to fill the holes for the contacts. Thickness must be at least half the diameter of contact.






## First metallization layer

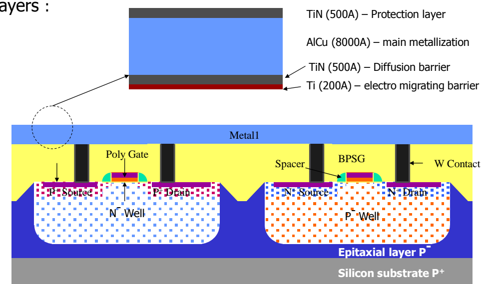
Polishing of Tungsten layer: CMP method. This step may have a planar surface. This removes the nitride Titan. The result is a jumper between the active components on the chip and the metallization layer of the future.






## First metallization layer

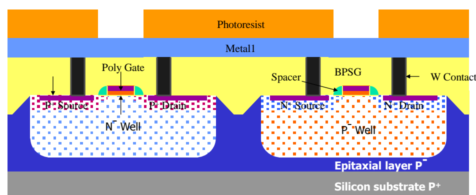
Deposition of Metalu1: Metallization is composed of several layers :






## First metallization layer

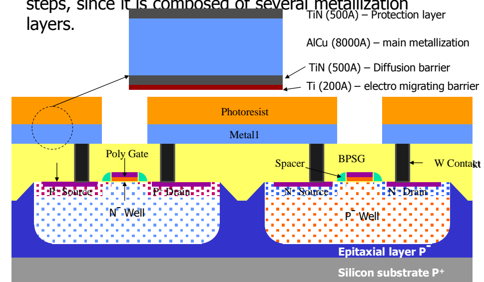
**Mask of METAL1**: Photoresist deposition and processing for the of the first layer of metallization





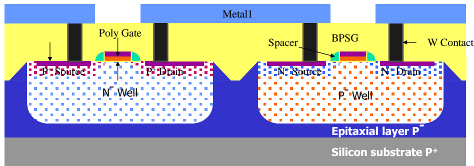

## First metallization layer

Etching of Metal1: RIE method. This is done in several steps, since it is composed of several metallization layers.



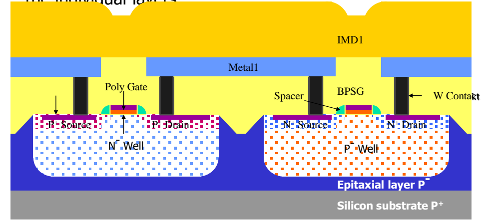
## First metallization layer

Photoresist removal: This step completes the first layer metallization.



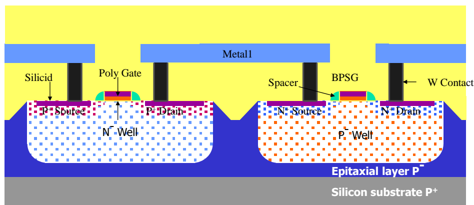
## The second to n-th layer metallization
**Today we have up to 11 layers !!!**

Deposition of IMD1: Non-subsidized silicon dioxide is deposited by CVD. Perfectly fills the gap between the metallization. Thickness of approximately one micrometer. This layer is used for electrical isolation of the individual layers.



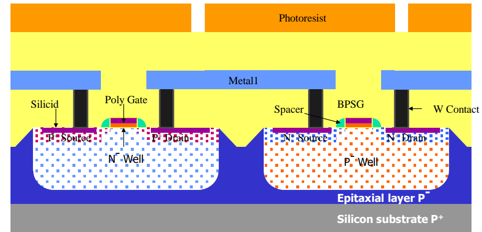
## The second to n-th layer metallization

Polishing of IMD1: Chemical-mechanical polishing ensures perfectly flat and smooth surface.



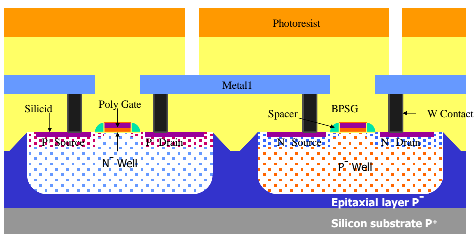
## The second to n-th layer metallization

**Mask of VIA1**: Application of and etching of photoresist.



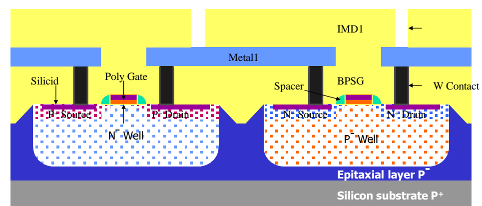
## The second to n-th layer metallization

Etching of VIA1: RIE.



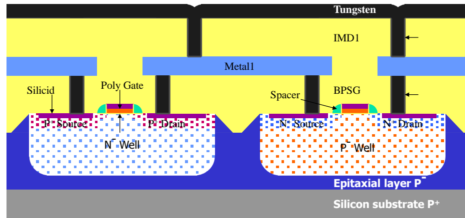
## The second to n-th layer metallization

Photoresist removal:



## The second to n-th layer metallization

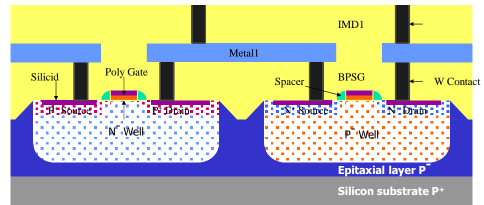
Deposition of Nitride and Titanium layer  - Tungsten: The same procedure as for the first metallization






## The second to n-th layer metallization

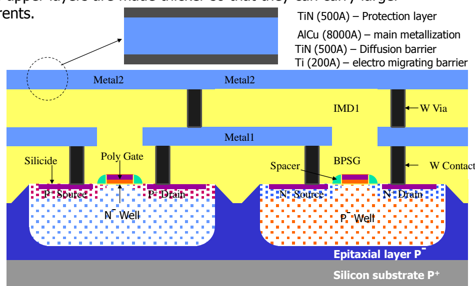
CMP:






## The second to n-th layer metallization

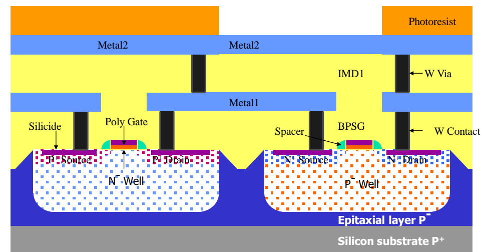
Deposition of Metal2:  A similar layers composition as in Metal1. The upper layers are made thicker so that they can carry larger currents.






## The second to n-th layer metallization

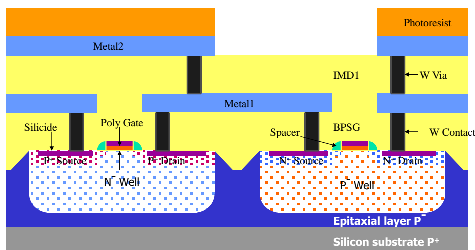
**Mask Metal2**:  Photoresist coating and developing.






## The second to n-th layer metallization

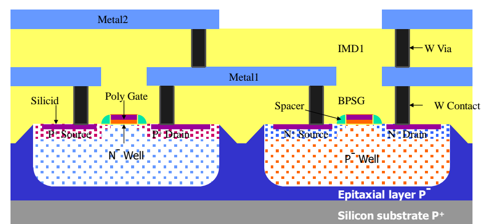
Metal2 etching:  RIE method. Must be done in a few steps.





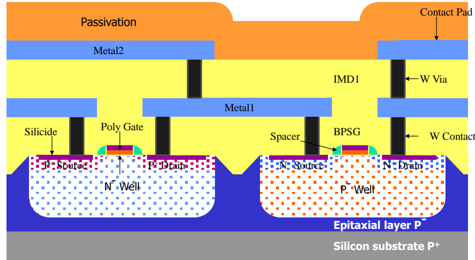

## The second to n-th layer metallization

Removal of photoresist: The second layer is complete



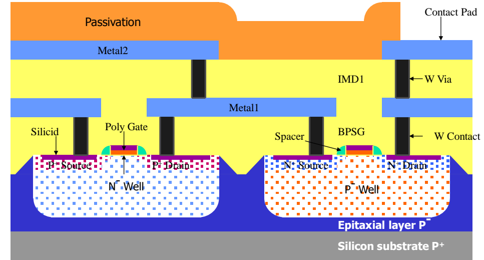
## Passivation

Deposition of passivation layers: There are many types of passivation layers (silicon nitrides, silicon oxynitride, polyimide, etc.). Their purpose is mechanical and chemical protection the the surface of the chip.





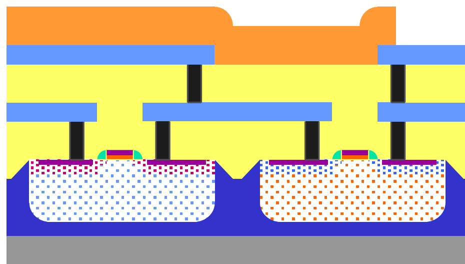

## Passivation





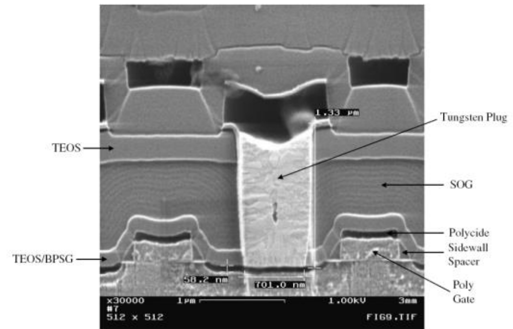

## CMOS technology

**Could you identify all layers ???**



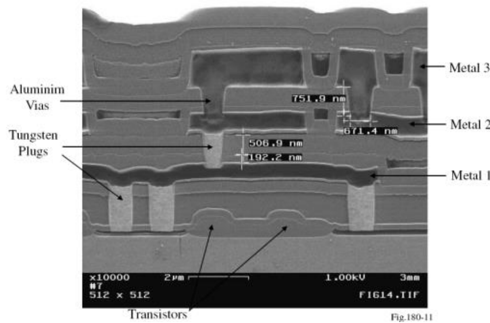


## Contact cross-section



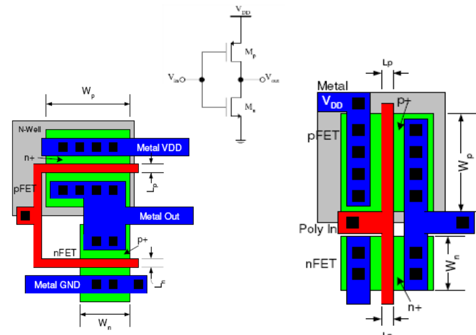



## Chip cross-section





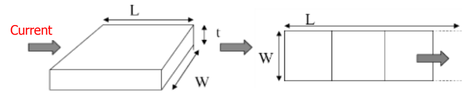

## Layout of CMOS invertor



# Passive components in IO structures

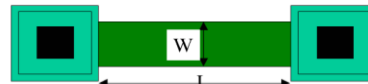
Resistors
Capacitors
Inductors

# Integrated resistor



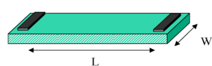

- Square resistance

$$R_{\square} = \rho/t \quad (\Omega/_{\square})$$




$$R \cong 2R_{contact} + (L/W)\, R_{\square}$$

# Integrated Resistors - Types and Properties

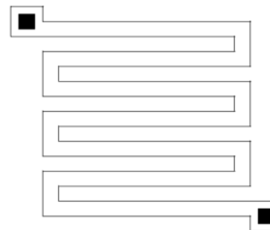



$$R = 2R_{cont} + \frac{L}{W} R_{\square}$$

| Type of layer | Sheet Resistance W/0 | Accuracy % | Temperature Coefficient ppm/°C | Voltage Coefficient ppm/V |
|---|---|---|---|---|
| n + diff | 30 - 50 | 20 - 40 | 200 - 1K | 50 - 300 |
| p + diff | 50 -150 | 20 - 40 | 200 - 1K | 50 - 300 |
| n - well | 2K - 4K | 15 - 30 | 5K | 10K |
| p - well | 3K - 6K | 15 - 30 | 5K | 10K |
| pinched n - well | 6K - 10K | 25 - 40 | 10K | 20K |
| pinched p - well | 9K - 13K | 25 - 40 | 10K | 20K |
| first poly | 20 - 40 | 25 - 40 | 500 - 1500 | 20 - 200 |
| second poly | 15 - 40 | 25 - 40 | 500 - 1500 | 20 - 200 |

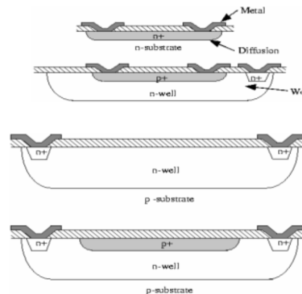
# Integrated resistors layout

Topology of the resistor



$$R = \frac{L}{W} R_{\square} = \frac{L}{W} \cdot \frac{\bar{\rho}}{x_j}$$

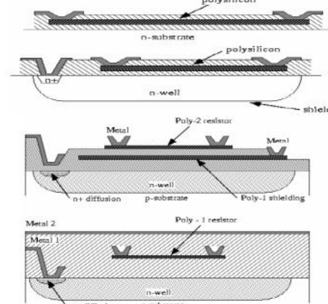
# Resistors realized by S and D field




Jsou realizovány pomocí difuzních oblastí

Pozor!
Jsou napěťově závislé

# Poly resistors

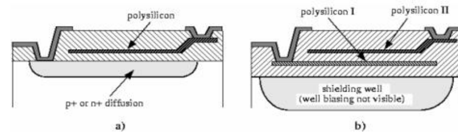


# Typical valued of PolyRes

| | Sheet Resistance (Ω/□) | Width Variation (µm ) (measured-drawn) | Contact Resistance (Ω) |
|---|---|---|---|
| **N+Actv** | 52.2 | -0.66 | 66.8 |
| **P+Actv** | 75.6 | -0.73 | 37.5 |
| **Poly** | 36.3 | -0.10 | 30.6 |
| **Poly 2** | 25.5 | 0.31 | 20.7 |
| **Mtl 1** | 0.05 | 0.56 | 0.05 |
| **Mtl 2** | 0.03 | -0.06 | |
| **N-Well** | 1513 | | |



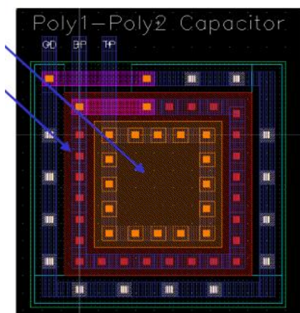
# Integrated capacitors




$$C = \frac{\varepsilon_{ox}}{t_{ox}} WL$$

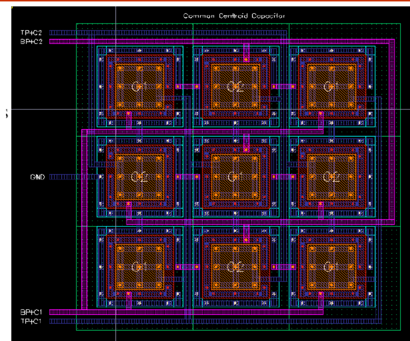


# Poly1 – Poly2 capacitor



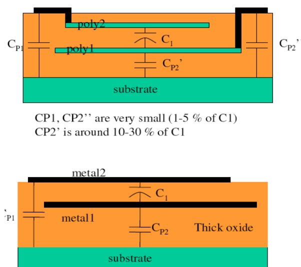


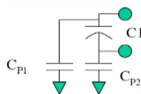

# Layout of IC capacitors






# Be aware of parasitic capacitors






# IC capacitors typical properties

| Capacitance | N+Actv | P+Actv | Poly | Poly 2 | Mtl 1 | Mtl 2 | UNITS |
|---|---|---|---|---|---|---|---|
| **Area (substrate)** | 292 | 290 | 35 | | 20 | 13 | aF/µm$^2$ |
| **Area (N+active)** | | | 1091 | 684 | 49 | 26 | aF/µm$^2$ |
| **Area (P+active)** | | | 1072 | 677 | | | aF/µm$^2$ |
| **Area (poly)** | | | | 599 | 45 | 23 | aF/µm$^2$ |
| **Area (poly2)** | | | **900** | | 45 | | aF/µm$^2$ |
| **Area (metal1)** | | | | | | 42 | aF/µm$^2$ |
| **Fringe (substrate)** | 80 | 170 | | | 36 | 25 | aF/µm |
| **Fringe (poly)** | | | | | 59 | 39 | aF/µm |